Administrative Stuff

- Homework 10 posted – just for practice. No need to turn in.
- Poster presentations tomorrow. No lecture. Sign up for time slot (office door of Prof. Rabaey). Poster template on web-site.
- Last lecture on Th – overview of future trends in digital IC design. Project 2 + Final discussion. Also HKN review. Your feedback is important!
Memory

Issues in Memory

- Memory Classification
- Memory Architectures
- The Memory Core
- Periphery
- Reliability
- Case Studies
## Semiconductor Memory Classification

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## Memory Timing: Definitions

![Memory Timing Diagram](image-url)
Memory Architecture: Decoders

Intuitive architecture for N x M memory
Too many select signals:
N words == N select signals

Decoder reduces the number of select signals
K = log₂N

Array-Structured Memory Architecture

Problem: ASPECT RATIO or HEIGHT >> WIDTH
Hierarchical Memory Architecture

Advantages:
1. Shorter wires within blocks
2. Block address activates only 1 block => power savings

Block Diagram of 4 Mbit SRAM

[Hirose90]
Read-Only Memory Cells

Diode ROM

MOS ROM 1

MOS ROM 2

MOS OR ROM

Pull-down loads

Vbias

VDD
**MOS NOR ROM**

Programming using the Active Layer Only

**MOS NOR ROM Layout**

Cell (9.5\(\lambda\) x 7\(\lambda\))
MOS NOR ROM Layout

Cell (11λ x 7λ)

Programming using the Contact Layer Only

- Polysilicon
- Metal1
- Diffusion
- Metal1 on Diffusion

MOS NAND ROM

All word lines high by default with exception of selected row

- WL[0]
- WL[1]
- WL[2]
- WL[3]

- BL[0] - BL[3]

- VDD

Pull-up devices
MOS NAND ROM Layout

Cell (8\(\lambda\) x 7\(\lambda\))

Programming using the Metal-1 Layer Only

No contact to VDD or GND necessary; drastically reduced cell size
Loss in performance compared to NOR ROM

Polysilicon
Diffusion
Metal1 on Diffusion

NAND ROM Layout

Cell (5\(\lambda\) x 6\(\lambda\))

Programming using Implants Only

Polysilicon
Threshold-altering implant
Metal1 on Diffusion
Equivalent Transient Model for MOS NOR ROM

Model for NOR ROM

- Word line parasitics
  - Wire capacitance and gate capacitance
  - Wire resistance (polysilicon)
- Bit line parasitics
  - Resistance not dominant (metal)
  - Drain and Gate-Drain capacitance

Equivalent Transient Model for MOS NAND ROM

Model for NAND ROM

- Word line parasitics
  - Similar to NOR ROM
- Bit line parasitics
  - Resistance of cascaded transistors dominates
  - Drain/Source and complete gate capacitance
Precharged MOS NOR ROM

PMOS precharge device can be made as large as necessary, but clock driver becomes harder to design.

Non-Volatile Memories
The Floating-gate transistor (FAMOS)

Device cross-section
Schematic symbol
Floating-Gate Transistor Programming

Avalanche injection
Removing programming voltage leaves charge trapped
Programming results in higher $V_T$.

A “Programmable-Threshold” Transistor

[Diagram showing a graph with two lines indicating programmable threshold]
**FLOTOX EEPROM**

Floating gate
Source
\( n^1 \)
Substrate
\( p \)
Gate
Drain
\( n^1 \)

20–30 nm
10 nm

FLOTOX transistor

Fowler-Nordheim
\( I-V \) characteristic

\(-10 \text{ V} \quad 10 \text{ V} \)

\( V_{GD} \)

**EEPROM Cell**

Absolute threshold control is hard
Unprogrammed transistor might be depletion
\( \Rightarrow 2 \text{ transistor cell} \)
Flash EEPROM

Control gate

Floating gate

Thin tunneling oxide

Many other options ...

Cross-sections of NVM cells

Flash

EPROM

Courtesy Intel
Basic Operations in a NOR Flash Memory—Erase

Basic Operations in a NOR Flash Memory—Write
Basic Operations in a NOR Flash Memory—Read

NAND Flash Memory
**NAND Flash Memory**

- Select transistor
- Word lines
- Active area
- STI
- Bit line contact
- Source line contact

Courtesy Toshiba

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**Read-Write Memories (RAM)**

- **STATIC (SRAM)**
  - Data stored as long as supply is applied
  - Large (6 transistors/cell)
  - Fast
  - Differential

- **DYNAMIC (DRAM)**
  - Periodic refresh required
  - Small (1-3 transistors/cell)
  - Slower
  - Single Ended
6-transistor CMOS SRAM Cell

CMOS SRAM Analysis (Read)

\[ k_{n,M5}(V_{DD} - \Delta V - V_{TH})V_{DSATn} - \frac{V_{DSATn}^2}{2} = k_{n,M1}(V_{DD} - V_{TH})\Delta V - \frac{\Delta V^2}{2} \]

\[ \Delta V = \frac{V_{DSATn} + CR(V_{DD} - V_{TH}) - \sqrt{V_{DSATn}^2 + CR^2(V_{DD} - V_{TH})^2}}{CR} \]
**CMOS SRAM Analysis (Read)**

\[ CR = \frac{W_1/L_1}{W_3/L_3} \]

**Voltage Rise (V)**

- 0
- 0.2
- 0.4
- 0.6
- 0.8
- 1
- 1.2
- 1.5
- 2
- 2.5
- 3

**Cell Ratio (CR)**

**CMOS SRAM Analysis (Write)**

\[ k_n_MD \left( V_{DD} - V_{Th} \right) V_Q - \frac{V_Q^2}{2} = k_{n,MD} \left( V_{DD} - |V_{Th}| \right) V_{DSAT} - \frac{V_{DSAT}^2}{2} \]

\[ V_Q = V_{DD} - V_{Th} - \left( V_{DD} - V_{Th} \right)^2 - \eta \frac{\mu_P}{\mu_n} \left( V_{DD} - |V_{Th}| \right) V_{DSAT} - \frac{V_{DSAT}^2}{2} \]
**CMOS SRAM Analysis (Write)**

![Graph showing the relationship between cell voltage and pull-up ratio.](image)

**6T-SRAM — Layout**

![Diagram of a 6T SRAM layout.](image)
Resistance-load SRAM Cell

Static power dissipation -- Want $R_L$ large
Bit lines precharged to $V_{DD}$ to address $t_p$ problem

3-Transistor DRAM Cell

No constraints on device ratios
Reads are non-destructive
Value stored at node $X$ when writing a “1” = $V_{WWL} - V_{Th}$
Write: $C_S$ is charged or discharged by asserting WL and BL.  
Read: Charge redistribution takes place between bit line and storage capacitance  

$$\Delta V = V_{BL} - V_{PRE} = V_{BIT} - V_{PRE} \frac{C_S}{C_S + C_{BL}}$$

Voltage swing is small; typically around 250 mV.
**DRAM Cell Observations**

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.
- DRAM memory cells are single ended in contrast to SRAM cells.
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design.
- When writing a “1” into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than $V_{DD}$.

**Sense Amp Operation**

Diagram showing the operation of a sense amp with $V_{BL}$, $V_{PRE}$, $V(0)$, and $V(1)$ over time $t$. The diagram illustrates the voltage changes at various points and the activation of the sense amp and word line.
**1-T DRAM Cell**

Cross-section

- Metal word line
- Poly
- Inversion layer induced by plate bias
- SiO$_2$
- Field Oxide

Layout

- Capacitor
- M$_1$ word line
- Diffused bit line
- Polysilicon gate
- Polysilicon plate

Uses Polysilicon-Diffusion Capacitance
Expensive in Area

**SEM of poly-diffusion capacitor 1T-DRAM**
Advanced 1T DRAM Cells

Trench Cell
- Cell Plate Si
- Capacitor Insulator
- Storage Node Poly
- 2nd Field Oxide
- Refilling Poly
- Si Substrate

Stacked-capacitor Cell
- Word line
- Insulating Layer
- Cell plate
- Capacitor dielectric layer
- Transfer gate
- Storage electrode
- Isolation