Administrative Stuff

- Homework 10 posted – just for practice. No need to turn in (hw 9 due today).
- Normal office hours next week.
- HKN review today. Your feedback is important!
- Final covers all material covered in class. Precise overview to be posted on web-site.
- Review session the day before the final (TBA)
Project 2 – some exciting results

- Most projects focused on non-restoring combined with mostly pass-transistor based implementation
- Some great alternatives
  - Look-up tables
  - Carry-select combined with concurrency
  - Exploit the specs …
- Grades:
  - Mean: 16.88
  - Median: 16.75
  - Stddev: 2.01
  - Max: 20

Memory
# Semiconductor Memory Classification

<table>
<thead>
<tr>
<th>Read-Write Memory</th>
<th>Non-Volatile Read-Write Memory</th>
<th>Read-Only Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Random Access</td>
<td>Non-Random Access</td>
<td>EPROM E²PROM</td>
</tr>
<tr>
<td>SRAM DRAM</td>
<td>FIFO</td>
<td>Flash</td>
</tr>
<tr>
<td></td>
<td>LIFO</td>
<td>Mask-Programmed</td>
</tr>
<tr>
<td></td>
<td>Shift Register</td>
<td>Programmable (PROM)</td>
</tr>
<tr>
<td></td>
<td>CAM</td>
<td></td>
</tr>
</tbody>
</table>

## 6-transistor CMOS SRAM Cell

[Diagram of 6-transistor CMOS SRAM Cell]

- **WL** (Word Line)
- **BL** (Bit Line)
- **M1-M6** Transistors
- **Q** Output
- **VDD** Power Supply
- **GND** Ground
**Resistance-load SRAM Cell**

Static power dissipation -- Want $R_L$ large
Bit lines precharged to $V_{DD}$ to address $t_p$ problem

**3-Transistor DRAM Cell**

No constraints on device ratios
Reads are non-destructive
Value stored at node $X$ when writing a “1” = $V_{WWL} - V_{Th}$
3T-DRAM — Layout

Write: CS is charged or discharged by asserting WL and BL.
Read: Charge redistribution takes place between bit line and storage capacitance

\[
\Delta V = \frac{C_S}{C_S + C_{BL}} \times (V_{PREF} - V_{PRE} - V_{BIT})
\]

Voltage swing is small; typically around 250 mV.
DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.
- DRAM memory cells are single ended in contrast to SRAM cells.
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design.
- When writing a “1” into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than $V_{DD}$.

Sense Amp Operation

![Diagram showing the operation of a sense amplifier.](EE141-S04)

- $V_{BL}$
- $V_{PRE}$
- $DV(1)$
- Word line activated
- Sense amp activated
- $V(0)$
- $V(1)$
**1-T DRAM Cell**

- **Cross-section**
  - Metal word line
  - Polysilicon gate
  - Polysilicon plate
  - Field Oxide
  - Diffused bit line
  - Capacitor

- **Layout**
  - M1 word line

**Uses Polysilicon-Diffusion Capacitance**
**Expensive in Area**

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**SEM of poly-diffusion capacitor 1T-DRAM**

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Advanced 1T DRAM Cells

Trench Cell
- Cell Plate Si
- Capacitor Insulator
- Storage Node Poly
- 2nd Field Oxide
- Si Substrate
- Refilling Poly

Stacked-capacitor Cell
- Word line
- Insulating Layer
- Cell plate
- Capacitor dielectric layer
- Transfer gate
- Isolation
- Storage electrode

EE 141 Summary

- Digital CMOS design is kicking and well
- Some major challenges down the road:
  - Cost
  - Power consumption
  - Robustness
  - Complexity
- Some new circuit solutions and design methodologies are bound to emerge
**18nm FinFET**

Double-gate structure + raised source/drain

X. Huang, et al, 1999
IEDM, p.67~70

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**And after that ...the nano-age??**

Organic (polymer)  
NEMS  
Nanotube  
Nano-contacts

Molecular

Quantum Dots
With ever more Exotic Behaviors ...  

Cost

- Mask cost in 90nm technology is over $1M
  - In 130nm is slowly dropping from 700k
- Bugs are very expensive
- Design effort increases in DSM
- Cost of new tools
- Non-recurring costs dominate the price effectiveness of low-volume ASICs
- Need to have a product that can fit multiple applications, customers (flexibility)
Power will be a problem

Power delivery and dissipation will be prohibitive

The Productivity Gap

Source: SEMATECH
From ASIC Design (Standard Cells)....

Cell-structure hidden under interconnect layers

To Flexible Solutions: RAM-based FPGA

Xilinx XC4025
**Xilinx Vertex-II**

18 embedded multipliers

3.1 Gbs Serial Interface

**Flexibility and Efficiency**

Flexibility

- Direct Mapped FPGA
- Embedded FPGA
- Reconfigurable Processor

Inefficiency (Power, Area)

- Embedded Processor (e.g. TI 320CXX)
- DSP
- 

**Xilinx Vertex-II**

- PowerPC 3.1 Gbs Serial Interface
- 18 embedded multipliers

**Flexibility and Efficiency**

- Direct Mapped FPGA
- Embedded FPGA
- Reconfigurable Processor

- Embedded Processor (e.g. TI 320CXX)
- DSP

Flexibility

Inefficiency (Power, Area)
The Challenge of the Next Decade

- The Deep Sub-Micron (DSM) Effect ($\leq 0.25\mu\text{m}$)

$\propto DSM$

"Microscopic Problems"
- Wiring Load Management
- Noise, Crosstalk
- Reliability, Manufacturability
- Complexity: LRC, ERC
- Accurate Power Prediction
- Accurate Delay Prediction
- etc.

Everything Looks a Little Different

$\propto 1/DSM$

"Macroscopic Issues"
- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

...and There’s a Lot of Them!

That’s all Folks

Thanks for the fun semester.
And … good luck in your future endeavors!