# Project 1

Due Friday, March 19th, 5pm @ 558 Cory

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<thead>
<tr>
<th>Name (Last, First)</th>
<th>Student ID</th>
<th>Design Group</th>
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<tr>
<th>Scoreboard</th>
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<td>Phase-1</td>
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<td>Phase-2</td>
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<tr>
<td>Phase-3</td>
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<td>Total (pts)</td>
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Background Information

You are given technology parameters that are essential in propagation delay analysis. These parameters are extracted by curve fitting simulated results of an inverter delay in our 0.25µm technology, as shown in Fig. 1.

![Figure 1: Extraction of delay parameters: (a) tp0, \( \gamma \), (b) V_on, \( \alpha_d \).](image)

(\( W_p/W_n=2\mu/1\mu, L=0.25\mu \))

Parameters \( t_{p0} \) and \( \gamma \) will aid in calculation of the gate delay as given by:

\[
t_p = t_{p0} \cdot \left(1 + \frac{f}{\gamma}\right)
\]

(1)

where \( t_{p0} \) is the intrinsic delay of an inverter, \( f \) is the fanout, and \( \gamma = C_{\text{intrinsic}}/C_{\text{gate}} \) is the ratio of the input intrinsic to the input gate capacitance.

Parameters \( V_{on} \) and \( \alpha_d \) are intrinsically related, but not equal to the transistor threshold voltage and velocity saturation index. They are simply fitting parameters that provide the most accurate model of a FO4 inverter delay over a range of supply voltages. Fanout of four is chosen for calibration simply because it is the most typical fanout found in well-designed digital circuits. It also represents good average fanout, so we will use the same parameters for all other fanouts that we are going to encounter in this design project. Relationship between the propagation delay of a FO4 inverter and the power supply \( V_{dd} \) is given by:

\[
t_p = K_d \cdot \frac{V_{dd}}{(V_{dd} - V_{on})^{\alpha_d}}
\]

(2)

where \( K_d \) is another fitting parameter, but it is not crucial for our problem setup. It lumps some technology parameters including linearized delay capacitance. You will find equation (2) useful in \( V_{dd} \)-based optimizations.
Phase 1: Optimal Design

You have to design an 8-input decoder, which implements the following 256 functions:

\[ F_0 = \overline{ABCDEFGH}; F_1 = \overline{ABCDEFGH}; \ldots; F_{255} = \overline{ABCDEF} \]

You may assume that all 8 inputs (A, B, C, D, E, F, G, H) are available in non-inverted and inverted format.

![An 8 input decoder.](image)

First, find the implementation and sizing that leads to the minimum possible delay. You are free to choose the topology of the gate (types of gates, number of gates in sequence) – Bear in mind however the following constraints:

- The load on the input signal (that is, the input capacitance of your network) should not be larger than that of a minimum size inverter.
- Every output is loaded with a capacitance equal to 128 times the input capacitance of a minimum size inverter.
- Only static complementary CMOS gates can be used.
- Identical gates (that is, gates of the same type with the same inputs) can appear only ONE TIME. This means that gates should be shared between different paths if possible.

What is the value of \( D_{\text{min}} \) normalized to \( t_{p0} \) (it should be the same for all 256 outputs). What is the energy \( E_{\text{ref}} \) that corresponds to the minimum delay? Since the energy depends upon how many inputs are changing, consider only the case where one input changes state (from 0 to 1 or vice versa). Assume \( V_{DD} = V_{DD}^{\text{nom}} = 2.5V \). Express \( E_{\text{ref}} \) in terms of energy required to drive the input gate capacitance \( C_{\text{gate}} = 1 \) (call this number “1”, it is simply a reference case, you do not need value in fF in your calculations) of the first gate in the chain. Now, you obtained reference point \( (D_{\text{min}}, E_{\text{ref}}) \) for your optimizations.
Phase 2 – Minimizing the Delay Penalty

Assume now that you are required to reduce the energy by \{20,30,40\}\%.
For the newly specified energy, perform following three optimizations in order to minimize delay penalty of
the reference design.

a) Gate size (W)/topology optimization
What is the new topology and the device sizes that minimizes the delay penalty?
What is the achieved percent delay penalty, \(\text{DP}_W = 100(\text{D}_W/\text{D}_{\text{min}} - 1)\)?

b) Supply voltage (Vdd) optimization
What is the value of the new supply voltage, \(V_{\text{DDopt}}\)?
What is the achieved percent delay penalty, \(\text{DP}_{V_{\text{dd}}} = 100(\text{D}_{V_{\text{dd}}}/\text{D}_{\text{min}} - 1)\)?

Clearly show your design methodology and summarize all results in following Table:

Summary of results from Phase-1: \(\text{D}_{\text{min}} (\text{tp}_0) = \text{E}_{\text{ref}} = \)

<table>
<thead>
<tr>
<th>Opt. case</th>
<th>DP (%)</th>
<th>(V_{\text{DDopt}})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference</td>
<td>0%</td>
<td>2.5V</td>
</tr>
<tr>
<td>W</td>
<td></td>
<td>2.5V</td>
</tr>
<tr>
<td>Vdd</td>
<td></td>
<td></td>
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Phase 3: Verification in HSPICE

Using HSPICE, verify results of your optimizations from Phase I and II.

a) Obtain reference point \((\text{D}_{\text{min}}, \text{E}_{\text{ref}})\) in HSPICE. Is it different from what you expected?
\(\text{Hint}:\) To determine energy dissipated in driving the input gate capacitance in HSPICE verification, you may want to use some of the results from background section and/or use
HSPICE to estimate this energy.

b) Using parameters (gate size, \(V_{\text{DDopt}}\)) from Phase II, report achieved energy reduction \(\text{ER}\) and
achieved delay penalty \(\text{DP}\) for all three optimization cases. Normalize numbers relative to the reference case \((\text{D}_{\text{min}}, \text{E}_{\text{ref}})\) obtained by HSPICE in part (a) of Phase-2.
Comment on your results.

Summary of results from Phase-3:

<table>
<thead>
<tr>
<th>Reference</th>
<th>(\text{D}_{\text{min}}) (ps)</th>
<th>(\text{E}_{\text{ref}}) (Ein-1st stage)</th>
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</thead>
<tbody>
<tr>
<td>HSPICE</td>
<td>Phase-1</td>
<td>HSPICE Phase-1</td>
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<tr>
<td>Verification</td>
<td>(\text{ER} (%))</td>
<td>(\text{DP} (%))</td>
</tr>
<tr>
<td>HSPICE</td>
<td>Phase-2</td>
<td>HSPICE Phase-2</td>
</tr>
<tr>
<td>W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vdd</td>
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