Problem 1 – CMOS Gate Design and Implementation

a) Design \( F = A + B + CD \) in combinational CMOS logic using the least number of devices. Draw the schematics and size the transistors so that the worst case equivalent resistances are equal to that of a minimum sized 2/1 inverter. Which input pattern would give you the worst and best equivalent pull-up or pull-down resistance.

b) Draw the logic graph corresponding to the circuit and identify the Euler paths

c) Using the Euler paths you found to draw the stick diagram for the implementation. You don’t need to distinguish different widths in the stick diagram.

d) What is the logical effort (g) of each input?

Problem 2 – Logic and Logical Effort

a) Draw the schematic of the 3-input NAND gate, and size all transistors such that the worst-case delay is equal to that of a minimum sized 2/1 inverter. Find the logical effort (g) of the 3-input NAND gate.

b) For the logic path from node (A) to node (B) shown in the figure above, find the path branching effort, path electrical effort, path logical effort, and total path effort. What is the optimum effort per stage for minimizing delay?

c) Find the input capacitances \( \{ X, Y, Z, W, V \} \) necessary for each of the gates in the path in order to achieve the optimum effort per stage.