EE141-Fall 2004
Digital Integrated Circuits
Instructor: Borivoje Nikolić
TuTh 3:30-5
247 Cory

What is this class all about?
- Introduction to digital integrated circuits.
  - CMOS devices and manufacturing technology.
  - CMOS inverters and gates. Propagation delay, noise margins, and power dissipation.
  - Combinational and sequential circuits. Timing and clocking. Arithmetic, interconnect, and memories.
  - Design methodologies.
- What will you learn?
  - Understanding, designing, and optimizing digital circuits with respect to different quality metrics: cost, speed, power dissipation, and reliability.
  - Practical design using state-of-the-art tools.

Practical Information
- Instructor
  - Prof. Borivoje Nikolic
    570 Cory Hall, 643-6997, bora@eecs
    Office hours: Mo 10:30am-12pm, Th 3:00-4:00pm
- TAs:
  - Zhengya Zhang, zyzhang@eecs
    Office hours: W 2-3pm, 353 Cory
  - Bill Tsang, ctsang@eecs
    Office hours: M 4-5pm, 353 Cory
  - TBA
    Office hours: TBA
- Web page:
  http://bwrc.eecs.berkeley.edu/Classes/ICDesign/EE141_s06/

Discussions and Labs
- Discussion sessions
  - M 3-4pm, Zhengya Zhang, 293 Cory
  - W 3-4pm, Zhengya Zhang, 293 Cory
  - Same material in both sessions!
- Labs (353 Cory)
  - M 1-4pm, Bill Tsang
  - W 11am-2pm, TBA
  - F 2-5pm, Bill Tsang
- Please choose one lab session and stick with it!

Your EECS141 Week

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* Discussion sections will cover identical material

Class Organization
- 10 Assignments
- One design project with three phases
- Labs: 5 software, 1 hardware
- 2 midterms, 1 final:
  - Midterm 1: Thursday, March 2, evening
  - Midterm 2: Thursday, April 6, evening
  - Final: Wednesday, May 19, 12:30-3:30pm
Some Important Announcements

- Please don’t bring food/drinks to 353 Cory
- Please use the newsgroup for asking questions (ucb.class.ee141)
- Project is done in pairs
- Homework is done individually
- Don’t even think about cheating!

Grading Policy

- Homeworks: 10%
- Labs: 10%
- Projects: 20%
- Midterms: 30%
- Final: 30%

Class Material

- Class notes: Web page
- Lab Reader: Available on the web page!
- Check web page for the availability of tools

The Web Site

- Class and lecture notes
- Assignments and solutions
- Lab and project information
- Exams
- Many other goodies …
- The sole source of information
  - http://bwrc.eecs.berkeley.edu/icdesign/eecs141_s06
  - Print only what you need: Save a tree!

Software

- Cadence
  - Industry standard
  - Online tutorials
  - We discontinued the use of MicroMagic in this class
- HSPICE and IRSIM for simulation

Getting Started

- Assignment 1: Getting SPICE to work – see web-page
- Due next Thursday, January 26, 5pm
- NO discussion sessions or labs this week.
- First discussion sessions in Week 2
- First Software lab in Week 3
**Digital Integrated Circuits**
- Introduction: Issues in digital design
- The CMOS inverter
- Combinational logic structures
- Sequential logic gates
- Design methodologies
- Interconnect: R, L and C
- Timing
- Arithmetic building blocks
- Memories and array structures

**Introduction**
- Why is designing digital ICs different today than it was before?
- Will it change in future?

**The First Computer**
- The Babbage Difference Engine
  - 25,000 parts
  - cost: £17,470

**ENIAC - The First Electronic Computer (1946)**

**The Transistor Revolution**
- First transistor
  - Bell Labs, 1948

**The First Integrated Circuits**
- Bipolar logic
  - 1960's
- ECL 3-input Gate
  - Motorola 1966
**Intel 4004 Microprocessor**

- 2,300 transistors (12mm²)
- 740 KHz operation
- (10μm PMOS technology)

**Intel Pentium 4 Microprocessor**

- Intel, 2005.
- 125,000,000 transistors (112mm²)
- 3.8 GHz operation
- (90nm CMOS technology)

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**Moore’s Law**

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months.

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**Evolution in Complexity**

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**Transistor Counts**

- Doubles every 2 years
**Frequency Trends in Intel's Microprocessors**

Has been doubling every 2 years, but is now slowing down.

**Power Trends in Intel's Microprocessors**

Has been > doubling every 2 years.

Power delivery and dissipation will be prohibitive.

**Power Density**

Power density too high to keep junctions at low temperature.

**Not Only Microprocessors**

Cell Phone

Digital Cellular Market (Phones Shipped)


Units 48M 86M 162M 260M 435M

(data from Texas Instruments)

**Productivity Trends**

Complexity outpaces design productivity.

Source: ITRS Roadmap
Why Scaling?
- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years...
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Challenges in Digital Design

- \( \propto DSM \)
  - "Microscopic Problems"
    - Ultra-high speed design
    - Interconnect
    - Noise, Crosstalk
    - Reliability, Manufacturability
    - Power Dissipation
    - Clock distribution.

- \( \propto 1/DSM \)
  - "Macroscopic Issues"
    - Time-to-Market
    - Millions of Gates
    - High-Level Abstractions
    - Reuse & IP: Portability
    - Predictability
    - etc.

Everything Looks a Little Different
… and There’s a Lot of Them!

Design Abstraction Levels

This Class
- Introduces basic metrics for design of integrated circuits – how to measure delay, power, etc.
- Groups layout rectangles into transistors and wires
  - Transistors and wires into gates
  - Gates into functions
  - (Functional blocks into systems) – e.g. EECS150
- Need to verify that the assumptions are valid

Next Lecture
- Introduces basic metrics for design of integrated circuits – how to measure delay, power, cost, etc.
- Brief intro to IC manufacturing and design