**Concept of Logical Effort**

- Normalize gate delay to an inverter

\[
\frac{\text{Delay}}{\tau_{\text{INV}}} = \frac{\tau_{\text{gate}}}{\tau_{\text{INV}}} \left( C_{\text{out}}^{\text{inv}} + \gamma_{\text{gate}} C_{\text{in}}^{\text{inv}} \right)
\]

\[
\tau_{\text{INV}} \cdot \gamma_{\text{INV}} = t_{p,\text{INV}}
\]

\[
\tau_{\text{gate}} \cdot \gamma_{\text{gate}} = t_{p,\text{gate}}
\]

- Logical Effort
- Fanout
- “Electrical Effort”

\[
\frac{\tau_{\text{gate}}}{\tau_{\text{INV}}} \cdot \gamma_{\text{gate}} = \frac{R \cdot C_{g,\text{gate}}}{R \cdot C_{g,\text{inv}}} \cdot \frac{C_{\text{int,\text{gate}}}}{C_{\text{int,\text{inv}}}} \cdot \frac{C_{\text{int,INV}}}{C_{g,\text{INV}}} \cdot \frac{P}{\gamma_{\text{INV}}}
\]

- Parasitic Delay

**Logical Effort Formalism (1/4)**

- Gate delay we used up to now:

\[
\text{Delay} = 0.69 \cdot R_{\text{drive}} \cdot C_{\text{intrinsic}} \cdot \left( 1 + \frac{C_{\text{out}}}{\gamma \cdot C_{\text{in}}} \right) = t_{p,0} \left( 1 + \frac{C_{\text{out}}}{\gamma \cdot C_{\text{in}}} \right)
\]

- Another way to write this formula is:

\[
\text{Delay} = 0.69 \cdot R_{\text{drive}} \cdot C_{\text{gate}} \cdot \left( \gamma + \frac{C_{\text{out}}}{C_{\text{in}}} \right) = \tau_{\text{gate}} \cdot \left( \gamma + \frac{C_{\text{out}}}{C_{\text{in}}} \right)
\]
Logical Effort Formalism (2/4)

- In this example, the total delay is:
  \[
  \text{Delay} = \tau_{\text{NAND}} \left( \gamma_{\text{NAND}} + \frac{C_{j+1}}{C_j} \right) + \tau_{\text{INV}} \cdot \left( \gamma_{\text{INV}} + \frac{C_{j+2}}{C_{j+1}} \right) + \tau_{\text{NOR}} \cdot \left( \gamma_{\text{NOR}} + \frac{C_{j+3}}{C_{j+2}} \right)
  \]

- Normalized to the intrinsic time constant of INV:
  \[
  \frac{\text{Delay}}{\tau_{\text{INV}}} = \frac{\tau_{\text{NAND}}}{\tau_{\text{INV}}} \left( \gamma_{\text{NAND}} + \frac{C_{j+1}}{C_j} \right) + \frac{\tau_{\text{INV}}}{\tau_{\text{INV}}} \cdot \left( \gamma_{\text{INV}} + \frac{C_{j+2}}{C_{j+1}} \right) + \frac{\tau_{\text{NOR}}}{\tau_{\text{INV}}} \cdot \left( \gamma_{\text{NOR}} + \frac{C_{j+3}}{C_{j+2}} \right)
  \]

Courtesy: B. Murmann, Stanford

Logical Effort Formalism (3/4)

- Since it is hard to fit on the back of an envelope, we define new symbols:
  \[
  \frac{\text{Delay}}{\tau_{\text{INV}}} = \frac{\tau_{\text{NAND}}}{\tau_{\text{INV}}} \cdot \left( \frac{C_{j+1}}{C_j} + \gamma_{\text{NAND}} \right) + \frac{\tau_{\text{INV}}}{\tau_{\text{INV}}} \cdot \left( \frac{C_{j+2}}{C_{j+1}} + \gamma_{\text{INV}} \right) + \frac{\tau_{\text{NOR}}}{\tau_{\text{INV}}} \cdot \left( \frac{C_{j+3}}{C_{j+2}} + \gamma_{\text{NOR}} \right)
  \]

  \[D = (g_{\text{NAND}} \cdot f_j + p_{\text{NAND}}) + (g_{\text{INV}} \cdot f_{j+1} + p_{\text{INV}}) + (g_{\text{NOR}} \cdot f_{j+2} + p_{\text{NOR}})\]

Logical Effort \quad \text{Parasitic Delay}

“Electrical Effort”
Logical Effort Formalism (4/4)

More nomenclature:
- \( D_{gate} = g \cdot f + p = h + p \)
  = Effort Delay + Parasitic Delay

Some options to find LE of a logic gate:
- Set \( R_{drive} \) equal, then compare \( C_{in} \)
- Set \( C_{in} \) equal, then compare \( R_{drive} \)
- Or simply compare \( R \) and \( C \) ratio from first principles:

\[
g_{gate} = \frac{\tau_{gate}}{\tau_{INV}} = \frac{(R_{drive} \cdot C_{in})_{gate}}{(R_{drive} \cdot C_{in})_{INV}}
\]

1: Calculating Logical Effort

**DEF:** Logical effort is the ratio of the input capacitance to the input capacitance of an inverter delivering the same output current

**Reference**

**Inverter:**
- \( C_{in} = 3 \)
- \( LE = 1 \) (def)

**NAND2:**
- \( C_{in} = 4 \)
- \( LE = 4/3 \)

**NOR2:**
- \( C_{in} = 5 \)
- \( LE = 5/3 \)
DEF: Parasitic delay is the ratio of intrinsic capacitance at the output and intrinsic capacitance at the output of an equivalent inverter.

**2: Calculating Parasitic Delay**

**Inverter:**
\[ C_{int} = 3 \]
\[ P = 1 \ (\text{def}) \]

**NAND2:**
\[ C_{int} = 6 \]
\[ P = 2 \]

**NOR2:**
\[ C_{int} = 6 \]
\[ P = 2 \]

**Reference**

*Source: "Logical Effort," I. Sutherland, B. Sproull, D. Harris (Morgan-Kaufmann 1999)*

**LE Catalog of Gates**

<table>
<thead>
<tr>
<th>Gate type</th>
<th>Number of inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td>inverter</td>
<td>1</td>
</tr>
<tr>
<td>NAND</td>
<td>4/3</td>
</tr>
<tr>
<td>NOR</td>
<td>5/3</td>
</tr>
<tr>
<td>multiplexer</td>
<td>2</td>
</tr>
<tr>
<td>Muller C</td>
<td>2</td>
</tr>
<tr>
<td>xor (parity)</td>
<td>4</td>
</tr>
<tr>
<td>majority</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Gate type</th>
<th>Parasitic delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>inverter</td>
<td>( \text{Pin} )</td>
</tr>
<tr>
<td>n-input NAND</td>
<td>( n \text{Pin} )</td>
</tr>
<tr>
<td>n-input NOR</td>
<td>( n \text{Pin} )</td>
</tr>
<tr>
<td>n-way multiplexer</td>
<td>2( n \text{Pin} )</td>
</tr>
<tr>
<td>n-input Muller C</td>
<td>2( n \text{Pin} )</td>
</tr>
<tr>
<td>xor, xnor</td>
<td>4( n \text{Pin} )</td>
</tr>
<tr>
<td>3-input majority</td>
<td>6( n \text{Pin} )</td>
</tr>
</tbody>
</table>

*Source: "Logical Effort," I. Sutherland, B. Sproull, D. Harris (Morgan-Kaufmann 1999)*
**LE and P from Simulation Data**

- **Normalized delay**: $D = 4/3$
- **Effort Delay**: $P = 2$
- **Parasitic Delay**: $D = (4/3)f + 2$

**Logical Effort “Design Flow”**

- Compute the path effort: $\text{Path Effort} = \prod LE \cdot FO \cdot B$
- Find the best number of stages: $N^* \sim \log_4(\text{Path Effort})$
- Compute the stage effort: $h^* = (\text{Path Effort})^{1/N}$
- Working from either end, determine gate sizes:

$$C_{in} = g \cdot b \cdot \frac{C_{out}}{h^*}$$

*Reference: Sutherland, Sproull, Harris, “Logical Effort,” (Morgan-Kaufmann 1999)*