Announcements

- Project launch today
  - Phase 1 due March 20
- Homework #7 due next Thursday
  - No new homework next week
Class Material

- Last lecture
  - Design for speed
  - Method of logical effort
- Today’s lecture
  - SRAM design
- Reading (Chapter 12)
Array-Structured Memory Architecture

Semiconductor Memory Classification

<table>
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<tr>
<th>Read-Write Memory</th>
<th>Non-Volatile Read-Write Memory</th>
<th>Read-Only Memory</th>
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<tr>
<td>Random Access</td>
<td>Non-Random Access</td>
<td>EPROM</td>
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<td>SRAM, DRAM</td>
<td>FIFO</td>
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<td>LIFO</td>
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<td>Shift Register</td>
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<td>CAM</td>
<td>Mask-Programmed Programmable (PROM)</td>
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Read-Write Memories (RAM)

- **STATIC (SRAM)**
  - Data stored as long as supply is applied
  - Large (6 transistors/cell)
  - Fast
  - Differential

- **DYNAMIC (DRAM)**
  - Periodic refresh required
  - Small (1-3 transistors/cell)
  - Slower
  - Single Ended

Positive Feedback: Bi-Stability
**Meta-Stability**

Gain should be larger than 1 in the transition region.

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**Writing into a Cross-Coupled Pair**

Can implement as a transmission gate as well.
Access transistor must be able to overpower the feedback.
Complementary data values are written (read) from two sides

**6-transistor CMOS SRAM Cell**

Diagram of the 6-transistor CMOS SRAM cell with labels for transistors M₁, M₂, M₃, M₄, M₅, and M₆, and connections for signals WL, V_DD, Q, and BL.
**SRAM Operation**

**Write**

![Write diagram](image1)

**Hold**

![Hold diagram](image2)

**SRAM Operation**

**Read**

![Read diagram](image3)

Reading the cell should not destroy the stored value
CMOS SRAM Analysis (Read)

\[
k_{n,M2}\left(V_{DD} - \Delta V - V_{TN}\right) - \frac{V_{DSAT}}{2} = k_{n,M1}\left(V_{DD} - V_{TN}\right)\Delta V - \frac{\Delta V^2}{2}
\]

\[
\Delta V = \frac{V_{DSAT} + CR(V_{DD} - V_{TN}) - \sqrt{V_{DSAT}^2(1 + CR) + CR^2(V_{DD} - V_{TN})^2}}{CR}
\]
CMOS SRAM Analysis (Write)

\[ PR = \frac{(W/L)_4}{(W/L)_6} \]

\[ k_{x,M_0} \left( (V_{DD} - V_{t_h})V_0 - \frac{V_0^2}{2} \right) = k_{p,M_1} \left( (V_{DD} - |V_{t_p}|)V_{D\text{SAT}_p} - \frac{V_{D\text{SAT}_p}^2}{2} \right) \]

\[ V_0 = V_{DD} - V_{t_n} - \sqrt{V_{DD} - V_{t_p}^2} - \frac{2 \mu C_{ox} P_{R}(V_{DD} - |V_{t_p}|)V_{D\text{SAT}_p} - \frac{V_{D\text{SAT}_p}^2}{2}}{2} \]

CMOS SRAM Analysis (Write)
Static Noise Margin

Obtained by breaking the feedback between the inverters

6T-SRAM — Layout

Compact cell
Bitlines: M2
Wordline: bootstrapped in M3
**65nm SRAM**

- ST/Philips/Motorola

Access Transistor

- Pull down
- Pull up

**Next Lecture**

- Alternate static logic styles
- Pass-transistor logic