Lecture 20
Domino Logic

Administrative Stuff

- Homework #8 due Thursday, April 6
- Project phase 2 due on Monday, April 3
  - Report template posted on the web
- Midterm 2 coming up
  - Thursday, April 6, 6:30-8pm, 277 Cory
  - Review session on Monday, April 3
- No lecture on Tuesday, April 4.
  - Lecture on Thursday, April 6.
Class Material

- Last lecture
  - Finished pass-transistor logic
  - Dynamic logic
- Today’s lecture
  - Domino logic
  - Bitline design
  - Power
- Reading
  - Chapter 6

Domino Logic
### Cascading Dynamic Gates

Only $0 \rightarrow 1$ transitions allowed at inputs!

### Domino Logic
**Why Domino?**

Like falling dominos!

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**Properties of Domino Logic**

- Only non-inverting logic can be implemented
- Very high speed
  - static inverter can be skewed, only L-H transition
  - Input capacitance reduced – smaller logical effort
Designing with Domino Logic

The first gate in the chain needs a foot switch
Precharge is rippling – short-circuit current
A solution is to delay the clock for each stage

Footless Domino
### Differential (Dual Rail) Domino

Solves the problem of non-inverting logic

### np-CMOS

Only $0 \rightarrow 1$ transitions allowed at inputs of PDN
Only $1 \rightarrow 0$ transitions allowed at inputs of PUN
**NORA Logic**

WARNING: Very sensitive to noise!

**Bitline Design**
**Bitline Design**

1. Bitline loads
   - Precharged (dynamic)
   - Clamped (static)
2. Write circuit
   - Inputs and outputs are separated
   - Writing 0 – use an NMOS pass transistor
3. Read circuit
   - Reading high voltages – use PMOS
   - Voltage or current sensing
   - Bitlines are often multiplexed
     - Large sense amps are hard to fit into a bitline pitch

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**Bitline Design**

- Pre-charged bitlines
  - Option: static (clamped) pull-up
- Voltage sensing
- Separate input and output
**Latch-Based Sense Amplifier**

Initialized in its meta-stable point with EQ
Once adequate voltage gap created, sense amp enabled with SE
Positive feedback quickly forces output to a stable operating point.

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**Power Revisited**
Transition Activity and Power

- Energy consumed in $N$ cycles, $E_N$:

$$E_N = C_L \cdot V_{DD}^2 \cdot n_{0\rightarrow1}$$

- $n_{0\rightarrow1}$ – number of $0\rightarrow1$ transitions in $N$ cycles

$$P_{avg} = \lim_{N \to \infty} \frac{E_N}{N} \cdot f = \lim_{N \to \infty} \frac{n_{0\rightarrow1}}{N} \cdot C_L \cdot V_{DD}^2 \cdot f$$

$$\alpha_{0\rightarrow1} = \lim_{N \to \infty} \frac{n_{0\rightarrow1}}{N} \cdot f$$

$$P_{avg} = \alpha_{0\rightarrow1} \cdot C_L \cdot V_{DD}^2 \cdot f$$

Factors Affecting Transition Activity

- “Static” component (does not account for timing)
  - Type of Logic Function (NOR vs. XOR)
  - Type of Logic Style (Static vs. Dynamic)
  - Signal Statistics
  - Inter-signal Correlations

- “Dynamic” or timing dependent component
  - Circuit Topology
  - Signal Statistics and Correlations
Type of Logic Function: NOR vs. XOR

Example: Static 2-input NOR Gate

Assume signal probabilities
\[ p_{A=1} = 1/2 \]
\[ p_{B=1} = 1/2 \]

Then transition probability
\[ p_{0\rightarrow1} = p_{\text{Out}=0} \times p_{\text{Out}=1} \]
\[ = 3/4 \times 1/4 = 3/16 \]

If inputs switch every cycle
\[ \alpha_{0\rightarrow1} = 3/16 \]

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Type of Logic Function: NOR vs. XOR

Example: Static 2-input XOR Gate

Assume signal probabilities
\[ p_{A=1} = 1/2 \]
\[ p_{B=1} = 1/2 \]

Then transition probability
\[ p_{0\rightarrow1} = p_{\text{Out}=0} \times p_{\text{Out}=1} \]
\[ = 1/2 \times 1/2 = 1/4 \]

If inputs switch in every cycle
\[ \alpha_{0\rightarrow1} = 1/4 \]
**Power Consumption of Dynamic Gates**

Power only dissipated when previous Out = 0

**Dynamic Power Consumption is Data Dependent**

Dynamic 2-input NOR Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
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<td>0</td>
</tr>
</tbody>
</table>

Assume signal probabilities

\[
P_{A=1} = 1/2 \quad P_{B=1} = 1/2
\]

Then transition probability

\[
P_{0\rightarrow1} = P_{\text{out}=0} \times P_{\text{out}=1} = 3/4 \times 1 = 3/4
\]

Switching activity always higher in dynamic gates!

\[
P_{0\rightarrow1} = P_{\text{out}=0}
\]
**Dynamic CVSL**

Guaranteed transition for every operation!

\[ \alpha_{0 \rightarrow 1} = 1 \]

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**Clock**

- Always switches
- Consumes 25-50% of power
- Clock gating commonly employed
**Problem: Reconvergent Fanout**

\[ P(Z = 1) = P(B = 1) \cdot P(X = 1 \mid B=1) \]

Becomes complex and intractable fast

**Inter-Signal Correlations**

- Logic without reconvergent fanout:
  \[ p_{0 \rightarrow 1} = (1 - p_A p_B) \cdot p_A p_B \]

- Logic with reconvergent fanout:
  \[ P(Z = 1) = p(C=1 \mid B=1) \cdot p(B=1) \]
  \[ p_{0 \rightarrow 1} = 0 \]

- Need to use conditional probabilities to model inter-signal correlations
- CAD tools required for such analysis
**Glitching in Static CMOS**

The result is correct, but there is extra power dissipated.

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**Example: Chain of NOR Gates**

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**Principles for Power Reduction**

- **Prime choice: Reduce voltage!**
  - Recent years have seen an acceleration in supply voltage reduction
  - Design at very low voltages still open question
  - Reducing thresholds to improve performance increases leakage
- **Reduce switching activity**
- **Reduce physical capacitance**

**Next Lecture**

- **Digital arithmetic**
  - Datapath design
  - Adders