EE141-Spring 2006
Digital Integrated Circuits

Lecture 20
Domino Logic

Administrative Stuff
- Homework #8 due Thursday, April 6
- Project phase 2 due on Monday, April 3
  - Report template posted on the web
- Midterm 2 coming up
  - Thursday, April 6, 6:30-8pm, 277 Cory
  - Review session on Monday, April 3
- No lecture on Tuesday, April 4.
  - Lecture on Thursday, April 6.

Class Material
- Last lecture
  - Finished pass-transistor logic
  - Dynamic logic
- Today's lecture
  - Domino logic
  - Bitline design
  - Power
- Reading
  - Chapter 6

Domino Logic

Cascading Dynamic Gates
Only 0 → 1 transitions allowed at inputs!
Why Domino?

Like falling dominos!

Properties of Domino Logic

- Only non-inverting logic can be implemented
- Very high speed
  - Static inverter can be skewed, only L-H transition
  - Input capacitance reduced – smaller logical effort

Designing with Domino Logic

Inputs = 0 during precharge

Can be eliminated!

Footless Domino

The first gate in the chain needs a foot switch
Precharge is rippling – short-circuit current
A solution is to delay the clock for each stage

Differential (Dual Rail) Domino

Solves the problem of non-inverting logic

np-CMOS

Only 0 → 1 transitions allowed at inputs of PDN
Only 1 → 0 transitions allowed at inputs of PUN
NORA Logic

WARNING: Very sensitive to noise!

Bitline Design

1. Bitline loads
   - Precharged (dynamic)
   - Clamped (static)
2. Write circuit
   - Inputs and outputs are separated
   - Writing 0 – use an NMOS pass transistor
3. Read circuit
   - Reading high voltages – use PMOS
   - Voltage or current sensing
   - Bitlines are often multiplexed
   - Large sense amps are hard to fit into a bitline pitch

Pre-charged bitlines
   - Option: static (clamped) pull-up
   - Voltage sensing
   - Separate input and output

Latch-Based Sense Amplifier

Initialized in its meta-stable point with EQ
Once adequate voltage gap created, sense amp enabled with SE
Positive feedback quickly forces output to a stable operating point.

Power Revisited
Transition Activity and Power

- Energy consumed in $N$ cycles, $E_N$:
  \[ E_N = C_L \cdot V_{DD}^2 \cdot n_{0\to1} \]
  
  - $n_{0\to1}$: number of $0\to1$ transitions in $N$ cycles

\[ P_{avg} = \lim_{N \to \infty} \frac{E_N}{N} = \left( \lim_{N \to \infty} \frac{n_{0\to1}}{N} \right) \cdot C_L \cdot V_{DD}^2 \cdot f \]

\[ \alpha_{0\to1} = \lim_{N \to \infty} \frac{n_{0\to1}}{N} \cdot f \]

\[ P_{avg} = \alpha_{0\to1} \cdot C_L \cdot V_{DD}^2 \cdot f \]

Factors Affecting Transition Activity

- "Static" component (does not account for timing)
  - Type of Logic Function (NOR vs. XOR)
  - Type of Logic Style (Static vs. Dynamic)
  - Signal Statistics
  - Inter-signal Correlations
- "Dynamic" or timing dependent component
  - Circuit Topology
  - Signal Statistics and Correlations

Type of Logic Function: NOR vs. XOR

Example: Static 2-input NOR Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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</table>

Assume signal probabilities

- $p_{A=1} = 1/2$
- $p_{B=1} = 1/2$

Then transition probability

- $P_{0\to1} = P_{\text{Out}=0} \times P_{\text{Out}=1}$

\[ = \frac{3}{4} \times \frac{1}{4} = \frac{3}{16} \]

If inputs switch every cycle

- $\alpha_{0\to1} = 3/16$

Type of Logic Function: XOR vs. XOR

Example: Static 2-input XOR Gate

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- $p_{B=1} = 1/2$

Then transition probability

- $P_{0\to1} = P_{\text{Out}=0} \times P_{\text{Out}=1}$

\[ = \frac{1}{2} \times \frac{1}{2} = \frac{1}{4} \]

If inputs switch every cycle

- $\alpha_{0\to1} = 1/4$

Power Consumption of Dynamic Gates

Dynamic Power Consumption is Data Dependent

Dynamic 2-input NOR Gate

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Assume signal probabilities

- $p_{A=1} = 1/2$
- $p_{B=1} = 1/2$

Then transition probability

- $P_{0\to1} = P_{\text{Out}=0} \times P_{\text{Out}=1}$

\[ = \frac{3}{4} \times 1 = \frac{3}{4} \]

Switching activity always higher in dynamic gates!

- $P_{0\to1} = P_{\text{Out}=0}$

Power only dissipated when previous Out = 0
**Dynamic CVSL**

- Guaranteed transition for every operation!

\[ \alpha_{B \rightarrow 1} = 1 \]

**Clock**

- Always switches
- Consumes 25-50% of power
- Clock gating commonly employed

**Problem: Reconvergent Fanout**

- Becomes complex and intractable fast

\[ P(Z = 1) = P(B = 1) \cdot P(X = 1 \mid B = 1) \]

**Inter-Signal Correlations**

- Logic without reconvergent fanout
  \[ P(Z = 1) = (1 - p_A p_B) p^2 \]
- Logic with reconvergent fanout
  \[ P(Z = 1) = p(C = 1 \mid B = 1) \cdot P(B = 1) \]
  \[ p_{B \rightarrow 1} = 0 \]

- Need to use conditional probabilities to model inter-signal correlations
- CAD tools required for such analysis

**Glitching in Static CMOS**

- The result is correct, but there is extra power dissipated

**Example: Chain of NOR Gates**

- Also known as dynamic hazards

- Gate Delay

<table>
<thead>
<tr>
<th>Time (ps)</th>
<th>Voltage (V)</th>
</tr>
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<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>200</td>
<td>0.5</td>
</tr>
<tr>
<td>600</td>
<td>0</td>
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Principles for Power Reduction

- Prime choice: Reduce voltage!
  - Recent years have seen an acceleration in supply voltage reduction
  - Design at very low voltages still open question
  - Reducing thresholds to improve performance increases leakage
- Reduce switching activity
- Reduce physical capacitance

Next Lecture

- Digital arithmetic
  - Datapath design
  - Adders