EE141-Spring 2006
Digital Integrated Circuits

Lecture 22
Sequential Logic Timing

Administrative Stuff
- Homework #9 due next Thursday
- Visit to Intel, April 21
  - Signup sheet
- Project phase 3 due on Monday, April 17
  - Report template posted on the web
- Midterm 2 – good job:
  - Hi: 46
  - Lo: 4
  - Median: 32
Class Material

- Last lecture
  - Power
  - Sequential logic
- Today’s lecture
  - Sequential logic
  - Timing
- Reading
  - Chapter 7

Sequential Logic
More Precise Setup Time

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)
**Setup-Hold Time Illustrations**

Hold-1 case

- Clk-Q Delay
- Time
- Clock
- Data

Keepers should be added to staticize

**Other Latches/Registers: C²MOS**
Other Latches/Registers: TSPC

Positive latch (transparent when CLK= 1)

Negative latch (transparent when CLK= 0)
Including Logic in TSPC

Example: logic inside the latch

AND latch

TSPC Register
Pulse-Triggered Latches

Ways to design an edge-triggered sequential cell:

Master-Slave Latches

Pulse-Triggered Latch

Pulsed Latches

(a) register

(b) glitch generation

(c) glitch clock
Pulsed Latches

Hybrid Latch – Flip-flop (HLFF), AMD K-6 and K-7:

CLK

D

P1

M1

M2

M3

M4

P2

P3

Q

M5

M6

CLKD
**HLFF Timing**

- **Volts**
  - 0.0
  - 0.2
  - 0.4
  - 0.6
  - 0.8
  - 1.0

**Time (ns)**

- 0.0
- 0.2
- 0.4
- 0.6
- 0.8
- 1.0

**Other Sequential Circuits**
Other Sequential Circuits

- Schmitt Trigger
- Monostable Multivibrators
- Astable Multivibrators

Schmitt Trigger

- VTC with hysteresis
- Restores signal slopes
Noise Suppression using Schmitt Trigger

CMOS Schmitt Trigger

Moves switching threshold of the first inverter
**Schmitt Trigger: Simulated VTC**

The effect of varying the ratio of the PMOS device $M_4$. The width is $k*0.5\mu m$.

**CMOS Schmitt Trigger (2)**

In $V_{DD}$

$M_4$

$M_3$

$M_2$

$M_1$

$M_6$

$X$

$M_5$

$V_{DD}$

$In$ $Out$
Multivibrator Circuits

- **Bistable Multivibrator**
  - flip-flop, Schmitt Trigger
- **Monostable Multivibrator**
  - one-shot
- **Astable Multivibrator**
  - oscillator

Transition-Triggered Monostable
Monostable Triggered (RC-based)

(a) Trigger circuit.

(b) Waveforms.

Astable Multivibrators (Oscillators)

simulated response of 5-stage oscillator