Lecture 24
Timing

Administrative Stuff

- Homework #9 due next Thursday
- Visit to Intel, April 21
  - Signup sheet
  - Friday lab - project ph. 4 starts after we get back
- Project phase 3 due on Monday, April 17
  - Report template posted on the web
- Project phase 4
  - In lab April 21-April 27
- Hardware lab next week
  - Friday section on April 28
Class Material

- Last lecture
  - Sequential logic
- Today’s lecture
  - Timing
- Reading
  - Chapter 7, 10

Timing Definitions
**Synchronous Timing**

![Diagram of synchronous timing]

**Latch Parameters**

![Diagram of latch parameters]

*Delays can be different for rising and falling data transitions*
**Register Parameters**

Delays can be different for rising and falling data transitions.

**Timing Constraints**

Cycle time: \( T_{\text{clk}} > t_{\text{c-q}} + t_{\text{logic}} + t_{\text{su}} \)

Race margin: \( t_{\text{hold}} < t_{\text{c-q,cd}} + t_{\text{logic,cd}} \)
Clock Nonidealities

- **Clock skew**
  - Spatial variation in temporally equivalent clock edges; deterministic + random, $t_{SK}$

- **Clock jitter**
  - Temporal variations in consecutive edges of the clock signal; modulation + random noise
  - Cycle-to-cycle (short-term) $t_{JS}$
  - Long term $t_{JL}$

- **Variation of the pulse width**
  - Important for level sensitive clocking

Clock Uncertainties

Sources of clock uncertainty

- Power Supply
- Interconnect
- Capacitive Load
- Temperature
- Coupling to Adjacent Lines
- Devices
- Clock Generation
Both skew and jitter affect the effective cycle time
Only skew affects the race margin
Positive and Negative Skew

(a) Positive skew

(b) Negative skew

Positive Skew

Launching edge arrives before the receiving edge
**Negative Skew**

Receiving edge arrives before the launching edge

**Timing Constraints**

Minimum cycle time:

\[ T - \delta = t_{c-q} + t_{su} + t_{logic} \]

Worst case is when receiving edge arrives early (positive \( \delta \))
### Timing Constraints

![Timing Constraints Diagram](image)

**Hold time constraint:**

\[ t_{(c-q, cd)} + t_{(logic, cd)} > t_{hold} + \delta \]

Worst case is when receiving edge arrives late
Race between data and clock

### Longest Logic Path in Edge-Triggered Systems

![Longest Logic Path Diagram](image)

Latest point of launching
Earliest arrival of next cycle
Clock Constraints in Edge-Triggered Systems

If launching edge is late and receiving edge is early, the data will not be too late if:

\[ T_{c-q} + T_{LM} + T_{SU} < T - T_{JI,1} - T_{JI,2} - \delta \]

Minimum cycle time is determined by the maximum delays through the logic

\[ T_{c-q} + T_{LM} + T_{SU} + \delta + 2 T_{JI} < T \]

Skew can be either positive or negative

Shortest Path

Earliest point of launching

Clk

Data must not arrive before this time

Nominal clock edge

Clk

EECS141
Clock Constraints in Edge-Triggered Systems

If launching edge is early and receiving edge is late:

\[ T_{c-q} + T_{LM} - T_{JI,1} < T_H + T_{JI,2} + \delta \]

Minimum logic delay

\[ T_{c-q} + T_{LM} < T_H + 2T_{JI} + \delta \]

How to counter Clock Skew?

Data and Clock Routing
**Flip-Flop – Based Timing**

- **Flip-flop** delay
- **Skew**
- **Logic delay**

\[
\phi = 1 \\
\phi = 0
\]

Representation after M. Horowitz, VLSI Circuits 1996.

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**Flip-Flops and Dynamic Logic**

- **Precharge**
- **Evaluate**

\[
\phi = 0 \\
\phi = 1
\]

Flip-flops are used only with static logic.
**Pipelining**

Reference Pipelining

<table>
<thead>
<tr>
<th>Clock Period</th>
<th>Adder</th>
<th>Absolute Value</th>
<th>Logarithm</th>
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<tbody>
<tr>
<td>1</td>
<td>(a_1 + b_1)</td>
<td></td>
<td></td>
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<tr>
<td>2</td>
<td>(a_2 + b_2)</td>
<td>(</td>
<td>a_2 + b_2</td>
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<td>4</td>
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<td>a_4 + b_4</td>
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<tr>
<td>5</td>
<td>(a_5 + b_5)</td>
<td>(</td>
<td>a_5 + b_5</td>
</tr>
</tbody>
</table>

**Latch-Based Pipeline**

Latch-Based Pipeline

Compute \(F\) compute \(G\)
Next Lecture

- Clock and power distribution