**EE141-Spring 2006**

**Digital Integrated Circuits**

Lecture 29
Flash memory

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**Administrative Stuff**

- Great job on projects and posters!
- Homework #10 due today
- Lab reports due this week
  - Friday lab in 353
- Final exam
  - May 19, 12:30-3:30pm 277 Cory

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**Class Material**

- Last lecture
  - Finish adders
  - ROM
- Today’s lecture
  - Flash memory
  - DRAM
- Reading
  - Chapter 12 (pp. 634-647, 664-670)

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**Flash Memory**

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**Read-Only Memory Cells**

- Diode ROM
- MOS ROM 1
- MOS ROM 2

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**MOS OR ROM**

- WL[0]
- WL[1]
- WL[2]
- WL[3]

- BL[0]
- BL[1]
- BL[2]
- BL[3]

- $V_{DD}$
- $V_{SS}$

- Pull-down loads
MOS NOR ROM Layout

Cell (9.5\(\lambda\) x 7\(\lambda\))

Programming using the Active Layer Only

- Polysilicon
- Metal1
- Diffusion
- Metal1 on Diffusion

Programmming using the Contact Layer Only

MOS NAND ROM Layout

Cell (11\(\lambda\) x 7\(\lambda\))

Programming using the Metal-1 Layer Only

Polysilicon
Metal1
Diffusion
Metal1 on Diffusion

No contact to VDD or GND necessary; drastically reduced cell size
Loss in performance compared to NOR ROM

NAND ROM Layout

Cell (5\(\lambda\) x 6\(\lambda\))

Programming using Implants Only

- Polysilicon
- Threshold-altering implant
- Metal1 on Diffusion
Equivalent Transient Model for MOS NOR ROM

Model for NOR ROM

- Word line parasitics
  - Wire capacitance and gate capacitance
  - Wire resistance (polysilicon)
- Bit line parasitics
  - Resistance not dominant (metal)
  - Drain and Gate-Drain capacitance

Equivalent Transient Model for MOS NAND ROM

Model for NAND ROM

- Word line parasitics
  - Similar to NOR ROM
- Bit line parasitics
  - Resistance of cascaded transistors dominates
  - Drain/Source and complete gate capacitance

Non-Volatile Memories
The Floating-gate transistor (FAMOS)

- Floating gate
- Source
- Gate
- Drain
- Substrate

Device cross-section
Schematic symbol

Floating-Gate Transistor Programming

- Avalanche injection
- Removing programming voltage leaves charge trapped
- Programming results in higher $V_T$

A “Programmable-Threshold” Transistor

- $I_D$ vs. $V_{GS}$
- “0”-state
- “1”-state
- $V_{WL}$
- $\Delta V_T$
- OFF

Flash EEPROM

- Control gate
- Floating gate
- Erasure
- Thin tunneling oxide
- Programming
- $n^+$ source
- $p$-substrate
- $n^+$ drain

Many other options ...
**Cross-sections of NVM cells**

Flash | EPROM
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**Basic Operations in a NOR Flash Memory—Erase**

**Basic Operations in a NOR Flash Memory—Write**

**Basic Operations in a NOR Flash Memory—Read**

**NAND Flash Memory**

**NAND Flash Memory**
**DRAM Cell Observations**

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.
- DRAM memory cells are single ended in contrast to SRAM cells.
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.
- When writing a “1” into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than VDD.

**Sense Amp Operation**

- The diagram shows the voltage swing (VBL) as a function of time (t).
- The voltage is referenced to VREF and VBL.

**1-T DRAM Cell**

- The cell uses polysilicon-diffusion capacitance, which is expensive in area.

**Modern 1T DRAM Cells**

- Trench Cell
- Stacked-capacitor Cell
THE END

- But this is just the beginning…