Updated Practical Information

- **Instructor**
  - Prof. Borivoje Nikolic
    - 570 Cory Hall, 643-9297, bora@eecs
    - Office hours: Mo 10:30am-12pm, Th 5:00-6:00pm

- **TAs:**
  - Zhengya Zhang, zy zzhang@eecs
    - Office hours: W 2-3pm, 353 Cory
  - Bill Tsang, ctsang@eecs
    - Office hours: M 4-5pm, 353 Cory
  - Seng Oon Toh, sengoon@eecs
    - Office hours: W 10-11am, 353 Cory
  - Luns Tee, luns@eecs
    - Office hours: Tu 2-3pm, 353 Cory
Updated Discussions and Labs

- **Discussion sessions**
  - M 3-4pm, Zhengya Zhang, 293 Cory
  - W 3-4pm, Zhengya Zhang, 521 Cory
  - Same material in both sessions!

- **Labs (353 Cory)**
  - M 1-4pm, Bill Tsang
  - W 11am-2pm, Seng
  - Th 12:30-3:30pm, Luns
  - F 2-5pm, Bill Tsang

- Please choose one lab session and stick with it!
  - A few people can move to Thursday discussion

Your EECS141 Week

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* Discussion sections will cover identical material
Announcements

- We are moving to 155 Donner Lab
  - From this Thursday, Feb 2
- Lab 2 this week!
  - No lab next week
  - Lab 3 in two weeks
- Homework #2 is due this Thursday
- Prof. Nikolic will not be holding office hours next week
  - Updated TA office hours on the web

Class Material

- Last lecture
  - CMOS manufacturing process
  - Design rules
- Today’s lecture
  - MOS transistor operation and modeling
- Reading (3.3.1-3.3.2)
Sticks Diagram

- Dimensionless layout entities
- Only topology is important

Stick diagram of inverter

Circuit Under Design

- Comprising transistors M1, M2, M3, and M4
- Input voltage $V_{in}$ connected to $V_{DD}$
- Output voltage $V_{out}$ connected to $V_{DD}$
- Other voltage levels indicated as $V_{out2}$
CMOS Inverter

Two Inverters

Share power and ground

Abut cells
Lab 2

2-input NAND gate

MOS Transistor
**What is a Transistor?**

A MOS Transistor \[\iff\] A Switch!

\[|V_{GS}| \geq |V_T|\]

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**Switch Model of MOS Transistor**

\[|V_{GS}| < |V_T|\]

\[|V_{GS}| > |V_T|\]
NMOS and PMOS

NMOS Transistor

PMOS Transistor

V_{GS} > 0

V_{GS} < 0

MOS Transistors: Types and Symbols

NMOS Enhancement

PMOS Enhancement

NMOS Depletion

NMOS with Bulk Contact
**Threshold Voltage: Concept**

![Diagram of a p-channel MOSFET](image)

**The Threshold Voltage**

- **Threshold**
  
  \[ V_T = V_{T0} + \gamma \cdot \left( \sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right) \]

- **Fermi potential**
  
  \[ \phi_F = \phi_T \cdot \ln \frac{N_A}{n_i} \]

2\(\phi_F\) is approximately \(-0.6V\) for p-type substrates
\(\gamma\) is the body factor
\(V_{T0}\) is approximately \(0.45V\) for our process
The Body Effect

Transistor in Linear Mode

V_{GS} > V_{DS} + V_T

V_{GS} \quad V_{DS} \quad I_D

S \quad G \quad D

n^+ \quad V(x) \quad n^+

L \quad x

p-substrate

B
The Drain Current

- Charge in the channel is controlled by the gate voltage:
  \[ Q_i(x) = -C_{ox} \cdot [V_{GS} - V(x) - V_T] \]
  \[ C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \]

- Drain current is proportional to charge and velocity:
  \[ I_D = -\nu_n(x) \cdot Q_i(x) \cdot W \]
  \[ \nu_n(x) = -\mu_n \cdot \xi(x) = \mu_n \cdot \frac{dV}{dx} \]

The Drain Current

- Combining velocity and charge:
  \[ I_D \cdot dx = \mu_n \cdot C_{ox} \cdot W \cdot (V_{GS} - V - V_T) \cdot dV \]

- Integrating over the channel:
  \[ I_D = k_n' \cdot \frac{W}{L} \cdot (V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \]

Transconductance: 
  \[ k_n' = \mu_n \cdot C_{ox} = \frac{\mu_n \cdot \varepsilon_{ox}}{t_{ox}} \]
**Transistor in Saturation**

$V_T < V_{GS} < V_{DS} + V_T$

![Diagram of transistor in saturation](image)

- **Pinch-off**

**Saturation**

- For $V_{GD} < V_T$, the drain current saturates:

$$I_D = \frac{k'n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

- Including channel-length modulation:

$$I_D = \frac{k'n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$$

**CLM**
**Modes of Operation**

Cutoff:

\[ V_{GS} < V_T \quad I_D = 0 \]

Resistive: (linear)

\[ V_{GS} > V_{DS} + V_T \quad V_{GS} > V_T \]

\[ I_D = k' \cdot \frac{W}{L} \cdot \left( V_{GS} - V_T \right) \cdot V_{DS} - \frac{V_{DS}^2}{2} \]

Saturation:

\[ V_T < V_{GS} < V_{DS} + V_T \]

\[ I_D = \frac{k' \cdot W}{L} \cdot (V_{GS} - V_T)^2 \]

**Current-Voltage Relations: A Good Ol' Transistor**

![Graph showing current-voltage relations with different VGS values](image)
A Model for Manual Analysis

\[ V_{DS} > V_{GS} - V_T \]

\[ I_D = \frac{k_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \]

\[ V_{DS} < V_{GS} - V_T \]

\[ I_D = k_n' \cdot \frac{W}{L} \cdot \left( (V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right) \]

with

\[ V_T = V_{T0} + \gamma \cdot \left( \sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|} \right) \]

Current-Voltage Relations:
The Deep Sub-Micron Transistor

![Graph showing current-voltage relations for different gate voltages.](image)
Velocity Saturation

- Velocity saturates due to carrier scattering effects

\[
\nu_n \quad (m/s) \\
\xi_c = 1.5 \\
\xi \quad (V/\mu m)
\]

- \(\nu_{sat} = 10^5\) (Constant velocity)
- Constant mobility (slope = \(\mu\))

Velocity Saturation

- ID

\[
I_D \\
V_{DSAT} \\
V_{GS} - V_T \\
V_{DS} \\
V_{GS} = V_{DD}
\]

- Long-channel device
- Short-channel device
$I_D$ versus $V_{GS}$

Long Channel (L=2.5μm)

Short Channel (L=0.25μm)

Regions of Operation

Long Channel (L=2.5μm)  W/L=1.5  Short Channel (L=0.25μm)
Including Velocity Saturation

Approximate velocity:

\[ v = \frac{\mu_n \xi}{1 + \xi/\xi_c} \quad \text{for} \quad \xi \leq \xi_c \]

\[ = v_{sat} \quad \text{for} \quad \xi \geq \xi_c \]

And integrate current again:

\[ I_D = \frac{\mu_n C_{ox}}{1 + (V_{DS}/\xi_c L)(W/L)} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \]

In deep submicron, there are four regions of operation:

1. cutoff, 2. resistive, 3. saturation and 4. velocity saturation

Regions of Operation

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
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<tr>
<td>V_{GS}: 2.5 V</td>
<td>I_D: 0.5 A</td>
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<tr>
<td>V_{GS}: 2.0 V</td>
<td>I_D: 0.3 A</td>
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<tr>
<td>V_{GS}: 1.5 V</td>
<td>I_D: 0.1 A</td>
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<tr>
<td>V_{GS}: 1.0 V</td>
<td>I_D: 0.05 A</td>
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Long Channel (L=2.5\,\mu m)  \quad W/L=1.5  \quad Short Channel (L=0.25\,\mu m)