Updated Practical Information
- **Instructor**
  - Prof. Borivoje Nikolic
  - 570 Cory Hall, 643-6997, bora@eecs
  - Office hours: Mo 10:30am-12pm, Th 5:00-6:00pm
- **TAs:**
  - Zhengya Zhang, zyzhang@eecs
    - Office hours: W 2-3pm, 353 Cory
  - Bill Tsang, ctsang@eecs
    - Office hours: M 4-5pm, 353 Cory
  - Seng Oon Toh, sengoon@eecs
    - Office hours: W 10-11am, 353 Cory
  - Luns Tee, luns@eecs
    - Office hours: Tu 2-3pm, 353 Cory

Updated Discussions and Labs
- **Discussion sessions**
  - M 3-4pm, Zhengya Zhang, 293 Cory
  - W 3-4pm, Zhengya Zhang, 293 Cory
  - Same material in both sessions!
- **Labs (353 Cory)**
  - M 1-4pm, Bill Tsang
  - W 11am-2pm, Seng
  - Th 12:30-3:30pm, Luns
  - F 2-5pm, Bill Tsang
- Please choose one lab session and stick with it!
  - A few people can move to Thursday discussion

Your EECS141 Week

Announcements
- We are moving to 155 Donner Lab
  - From this Thursday, Feb 2
- Lab 2 this week!
  - No lab next week
  - Lab 3 in two weeks
- Homework #2 is due this Thursday
- Prof. Nikolic will not be holding office hours next week
  - Updated TA office hours on the web

Class Material
- Last lecture
  - CMOS manufacturing process
  - Design rules
- Today’s lecture
  - MOS transistor operation and modeling
- Reading (3.3.1-3.3.2)
**Sticks Diagram**

- Dimensionless layout entities
- Only topology is important

**Circuit Under Design**

**CMOS Inverter**

**Two Inverters**

- Share power and ground
- Abut cells

**Lab 2**

**MOS Transistor**
What is a Transistor?

A MOS Transistor ↔ A Switch!

Switch Model of MOS Transistor

NMOS and PMOS

NMOS Transistor

PMOS Transistor

V_{GS} > 0

V_{GS} < 0

MOS Transistors: Types and Symbols

NMOS Enhancement

PMOS Enhancement

NMOS Depletion

NMOS with Bulk Contact

Threshold Voltage: Concept

The Threshold Voltage

Threshold

\[ V_T = V_{T0} + \gamma \cdot \left( \sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F} \right) \]

Fermi potential

\[ \Phi_F = \Phi \cdot \ln \frac{N_A}{n_i} \]

2\Phi_F is approximately –0.6V for p-type substrates

\gamma is the body factor

V_{T0} is approximately 0.45V for our process
The Drain Current
- Charge in the channel is controlled by the gate voltage:
  \[ Q(x) = -C_{ox} \left( V_{GS} - V(x) - V_T \right) \]
- Drain current is proportional to charge and velocity:
  \[ I_D = -v_n(x) \cdot Q(x) \cdot W \]
  \[ v_n(x) = -\mu_n \cdot \xi(x) = \mu_n \frac{dV}{dx} \]

Transistor in Saturation
- For \( V_{GD} < V_T \), the drain current saturates:
  \[ I_D = \frac{k'_n}{2} \frac{W}{L} \left( V_{GS} - V_T \right)^2 \]
- Including channel-length modulation:
  \[ I_D = \frac{k'_n}{2} \frac{W}{L} \left( V_{GS} - V_T \right)^2 \left( 1 + \lambda \cdot V_{DS} \right) \]

Transistor in Linear Mode
- \( V_{GS} > V_{DS} + V_T \)
- The drain current is proportional to charge and velocity:
  \[ I_D = \mu_n \cdot C_{ox} \cdot W \cdot (V_{GS} - V - V_T) \, dV \]
- Integrating over the channel:
  \[ I_D = k'_n \cdot \frac{W}{L} \left( V_{GS} - V_T \right) \cdot V_{DS} - \frac{V_{DS}^2}{2} \]
- Transconductance:
  \[ k'_n = \mu_n \cdot C_{ox} = \frac{\mu_n \cdot C_{ox}}{L_{ox}} \]
**Modes of Operation**

- **Cutoff:**
  \[ V_{gs} < V_t \]
  \[ I_D = 0 \]

- **Resistive:**
  \[ V_{gs} > V_{ds} + V_t \]
  \[ I_D = \frac{k_n}{2} \frac{W}{L} \left( V_{gs} - V_t \right)^2 \]

- **Saturation:**
  \[ V_f < V_{gs} < V_{ds} + V_t \]
  \[ I_D = \frac{k_n}{2} \frac{W}{L} \left( V_{gs} - V_t \right)^2 \]

**Current-Voltage Relations:**

**A Good Ol’ Transistor**

**A Model for Manual Analysis**

\[ I_D = \frac{k_n}{2} \frac{W}{L} \left( V_{gs} - V_t \right)^2 \left( 1 + \lambda \cdot V_{ds} \right) \]

**Current-Voltage Relations:**

**The Deep Sub-Micron Transistor**

- **Linear Relationship**
  \[ V_{ds} > V_{gs} - V_t \]
  \[ I_D = \frac{k_n}{2} \frac{W}{L} \left( V_{gs} - V_t \right)^2 \]

- **Saturation:**
  \[ V_{ds} < V_{gs} - V_t \]
  \[ I_D = \frac{k_n}{2} \frac{W}{L} \left( V_{gs} - V_t \right)^2 \left( 1 + \lambda \cdot V_{ds} \right) \]

**Velocity Saturation**

- Velocity saturates due to carrier scattering effects

\[ \nu_{sat} = 10^6 \]

**Velocity Saturation**

- **Constant velocity**
  \[ \nu_{sat} = 10^6 \]

- **Long-channel device**
  \[ V_{ds} = V_{dd} \]

- **Short-channel device**
  \[ V_{ds} = V_{sat} \]

- **Early Saturation**
  \[ V_{gs} = 2.5 V \]

- **Linear Relationship**
  \[ V_{gs} = 2.0 V \]

- **Saturation**
  \[ V_{gs} = 1.5 V \]

- **Quadratic Relationship**
  \[ V_{gs} = 1.0 V \]
Including Velocity Saturation

Approximate velocity:

\[ v = \frac{\mu_C V}{1 + \frac{V_{DS}}{V_T}} \quad \text{for} \quad \xi \leq \xi_c \]

\[ = v_{sat} \quad \text{for} \quad \xi \geq \xi_c \]

And integrate current again:

\[ I_D = \frac{\mu_C}{L} \left( \frac{V_{GS} - V_T}{V_D} \right) \left( V_{DS} - \frac{V_{DS}^2}{2} \right) \]

In deep submicron, there are four regions of operation:
1. cutoff,
2. resistive,
3. saturation and
4. velocity saturation.

Regions of Operation – Simplified

Define \( V_{GT} = V_{GS} - V_T \) and \( V_{DSAT} \approx L \xi_c^2 \)

A Unified Model for Manual Analysis

Define \( V_{GT} = V_{GS} - V_T \)

for \( V_{GT} \leq 0 \): \( I_D = 0 \)

for \( V_{GT} \geq 0 \):

\[ I_D = \frac{k}{L} \left( V_{GT} - V_{min} \right) \left( V_{GS} - V_{DSAT} \right) \]

with \( V_{min} = \min (V_{GT}, V_{DS}, V_{DSAT}) \)
Simple Model versus SPICE

Transistor Model for Manual Analysis

A PMOS Transistor

Next Lecture

- Using the MOS model:
  - Inverter VTC and delay