1. **SRAM bitline design**

In this phase, you will assemble (in both schematic and layout) a bitline consisting of 32 SRAM cells designed in phase I of the project (assuming that you broke the array in two halves; if you didn’t your bitline is 64 bits), together with peripheral circuitry as shown in Figure 1.

![Figure 1: SRAM column.](image-url)
Size the precharge, read and write access transistors to ensure read and write functionality of the column. Verify the DRC and LVS correctness of the design and simulate the write and read operation of the memory.

2. Sense Amplifier

Design the sense amplifier that uses positive feedback to amplify the difference of signals $Out$ and $\overline{Out}$, and achieve full-swing logic output. Enter the schematic, but you don’t need to do the layout.

Simulate the operation of the sense amplifier together with the extracted bitline column. The enable signal should rise when the difference between the bitlines achieves 100mV.

3. Report

The total report should not contain more than two pages. You are not allowed to add any other sheets. The organization of the report should be based on the following outline:

- Cover page: Names, project title
- Page 1: Annotated schematic and the layout of the SRAM bitline. Simulation of the read and write operation.
- Page 2: Annotated schematic of the sense amplifier. Simulation of the read operation.

Grading:

- 45% Approach and correctness
- 20% Results
- 30% Report
- 5% Creativity