1. We sometimes design the inverter to favor one transition. Fig 1 shows two examples with unequal rising and falling delays.

![Skewed inverters](image1)

(a) Figure 1 Skewed inverters.

(b) Figure 2 Clock distribution network.

(1) Calculate the logical effort of the skewed inverters shown in Fig. 1 for both rising and falling output transitions. Which inverter does favor rising output transition? Why? (10 pts)

(2) Suppose the skewed inverters shown in Fig. 1 are included in your digital cell library. Choose and design the inverter m1, m2, and m3 to minimize the delay Td for the low-to-high input transition, as shown in Fig. 2. Calculate the delay Td and the corresponding delay for the high-to-low input transition. (15 pts)

2. Following schematic implements the logic equation of (A+B+C+D). The four inverters connected to inputs are minimum sized.
(1) If $C_{load}$ is $25xC_{gmin}$, where $C_{gmin}$ is the gate capacitance of a minimum-size inverter. Size the NAND, NOR and INV gates to minimize the propagation delay from input to output. (10 pts)

(2) Repeat part (1) if $C_{load}$ is $1xC_{gmin}$. Be reminded that the input inverters are already minimum sized. Subsequent gates therefore cannot be smaller than unit size. (10 pts)

(3) Can you design another circuit that implements the same logic but has shorter propagation delay for the case of $C_{load}=1xC_{gmin}$? The four input inverters come from the I/O interface design. They can neither be replaced nor be resized. (10 pts)

3. Following schematic exemplifies a clock distribution network. The first inverter is of minimum size ($1\times$). Input capacitance of a minimum-size inverter is $C$. Also assume $\gamma=1$.

(1) Size the inverter $m1$ and $m2$ for the minimum delay. (5 pts)

(2) Assume all inverters share the same supply $Vdd$. What is the total energy drawn from the supply when the input switches from 0 to $Vdd$? What is the total energy dissipated as heat? (10 pts)