[PROBLEM 1] Elmore Delay

Part (b):

We assume $V_{DD} >> V_T$ or $V_T$ is very small (<0). You can ignore the threshold drops of those pass-transistor gates.

To simplify the calculation of the capacitances of the pass transistors, you may assume that $C_{gs}$ and $C_{gd}$ are constant when the transistor is on. (NOTE: This is just ONLY for simplification for hand analysis of this problem. In other real cases, $C_{gs}$ and $C_{gd}$ are different depending on the operation regions of the transistor.)

[PROBLEM 2] MOS Capacitance and Delay

This problem and its assumptions are very similar to the example in the textbook (page194~199). We encourage you to go through the content in the textbook and do an exercise of calculating capacitances in this problem.

Part(a):

we updated: "…. to calculate the equivalent $C_{int_{LH}}, C_{int_{HL}}, C_{ginv_{LH}},$ and $C_{ginv_{HL}}$ at node X.........."

[PROBLEM 3] MOS Capacitance and VTC revisited

Notation: To be consistent with lecture notes and hw#4, the notation, $V_{DSAT}$, is updated to $V_D, VSAT$

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The above minor updates are shown on the latest HW#5 revision. (by Stanley 2010/03/03)