Hw 6 posted.

Project phase 1 underway. Mail your group composition (list of names) to ee141@cory.eecs.berkeley.edu

No lecture on Fr
  - Make-up on Tu March 16 at 3:30pm
Class Material

- Last lecture
  - Optimizing complex logic
  - Pass transistor logic
- Today’s lecture
  - Pass transistor logic – continued
  - CMOS Layout
  - Pseudo-NMOS
- Reading (Ch 6)
Pass-Transistor Logic

- N transistors
- No static consumption

NMOS-Only Logic
**NMOS Only Logic: Level Restoring Transistor**

- Advantage: Full Swing
- Restorer adds capacitance, takes away pull down current at X
- Ratio problem

**Restorer Sizing**

- Upper limit on restorer size
- Pass-transistor pull-down can have several transistors in stack
Pass Transistor Logic LE

\[ C_{\text{pass}} = \quad R_{\text{pass}} = \quad L_{\text{pass}} = \]

Complementary Pass Transistor Logic

(a) Basic concept

(b) Example pass-transistor networks
CPL Level Restore

Solution 2: Transmission Gate
Resistance of Transmission Gate

![Graph showing resistance vs. V_out]

Pass-Transistor Based Multiplexer

![Diagram of pass-transistor based multiplexer]
Transmission Gate XOR

CMOS Layout
Complex CMOS Gate

\[
\text{OUT} = D + A \cdot (B + C)
\]

Cell Design

- **Standard Cells**
  - General purpose logic
  - Used to synthesize RTL/HDL
  - Same height, varying width

- **Datapath Cells**
  - For regular, structured designs (arithmetic)
  - Includes some wiring in the cell
Standard Cell Methodology

- Feedthrough cell
- Logic cell
- Rows of cells
- Functional module (RAM, multiplier, ...)
- Routing channel

Standard Cells – Then and Now

(a)  
(b)
Standard Cell Layout Methodology – 1990s - Today

No routing channels

M2

M3

Mirrored Cell

V_{DD}

V_{DD}

GND

GND

Cell boundary

N Well

Cell height 12 metal tracks

Metal track is approx. 3\lambda + 3\lambda

Pitch = repetitive distance between objects

Cell height is “12 Mn pitch”

Rails \sim 10\lambda
**Standard Cells**

With minimal diffusion routing

With silicided diffusion

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**Standard Cells**

2-input NAND gate
Stick Diagrams

Contains no dimensions
Represents relative positions of transistors

Inverter

\[ V_{DD} \]
\[ GND \]
\[ \text{In} \]
\[ \text{Out} \]

NAND2

\[ V_{DD} \]
\[ GND \]
\[ A \]
\[ B \]

Two Versions of \( C \cdot (A + B) \)

\[ A \]
\[ C \]
\[ B \]
\[ V_{DD} \]
\[ GND \]

\[ A \]
\[ B \]
\[ C \]
\[ V_{DD} \]
\[ GND \]
Logic Graphs

\[ X = C \cdot (A + B) \]

Consistent Euler Path

A B C  
Has PDN and PUN

B C A  
Has PUN, but no PDN
**OAI22 Logic Graph**

\[ X = (A+B)(C+D) \]

**Example: \( x = ab+cd \)**

(a) Logic graph for \((ab+cd)\)

(b) Euler paths \((ab\ c\ d)\)

(c) Stack diagram for ordering \((ab\ c\ d)\)
**Multi-Fingered Transistors**

One finger

Two fingers (folded)

Less diffusion capacitance

**Ratioed Logic**
Ratioed Logic

Goal: build gates faster/smaller than static complementary CMOS

Ratioed Logic LE

- Rising and falling delays aren’t the same
  - Calculate LE for the two edges separately

- For tpLH:
  - \( C_{gate} = W C_G \)
  - \( C_{inv} = (3/2)W C_G \)
  - \( LE_{LH} = \)
**Ratioed Logic LE (pull-down edge)**

- What is LE for \( t_{pHL} \)?
- Switch model would predict \( R_{\text{eff}} = R_n || R_p \)
  - Would that give the right answer for LE?

**Response on Falling Edge**

- Time constant is smaller, but it takes more time to complete 50% \( V_{DD} \) transient (arguably)
  - \( R_p \) actually takes some current away from discharging \( C \)
Ratioed Logic Pull-down Delay

- Think in terms of the current driving $C_{load}$

- When you have a conflict between currents
  - Available current is the difference between the two
  - In pseudo-nMOS case:
    \[
    R_{drive} = \frac{1}{R_n} - \frac{1}{R_p} \quad \rightarrow \quad R_{drive} = \frac{R_n}{1 - \left(\frac{R_n}{R_p}\right)}
    \]
  - (Works because $R_p \gg R_n$ for good noise margin)

Ratioed Logic LE (pull-down edge)

- For $t_{pHL}$ (assuming $R_{sqp} = 2R_{sqn}$):
  - $R_{gate} = R_n/(1-R_n/R_p) = 2R_n$
  - $R_{inv} = R_n$
  - $C_{gate} = WC_G$
  - $C_{inv} = 3WC_G$
  - $LE_{HL} =$

- LE is lower than an inverter!
  - But have static power dissipation…
**Improved Loads**

![Diagram of Improved Loads](image)

**Adaptive Load**

**Improved Loads (2)**

![Diagram of Improved Loads (2)](image)

**Differential Cascode Voltage Switch Logic (DCVSL)**
**DCVSL Transient Response**

**DCVSL Example 1: AND**
DCVSL Example2

XOR/XNOR gate