Administrativia

- Phase 2 announced. Launched in the next 24 hours.
- Hw 6 due on Fr.
Class Material

- Last lecture
  - Ratioed Logic
  - Dynamic Logic
- Today’s lecture
  - Domino Logic
  - Registers
- Reading (Ch 6, Ch 7)

Dynamic Logic
Phase 2 – Design the Bit Node

Goals: 
- Design bit-node so that clock frequency is minimized
- Layout bit and check nodes

Due Date: Wednesday April 13
Dynamic Gate

Two phase operation
- Precharge (Clk = 0)
- Evaluate (Clk = 1)

Challenges of Dynamic Gates
- Noise sensitivity and small noise margins
- Leakage
- Charge sharing
- Clock feedthrough
**Issues in Dynamic Design 3: Clock Feedthrough**

Coupling between Out and Clk input of the precharge device due to the gate to drain capacitance. So voltage of Out can rise above V_{DD}. The fast rising (and falling edges) of the clock couple to Out.

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**Clock Feedthrough**

Clock feedthrough

Clock feedthrough
Issues in Dynamic Design 4: Backgate Coupling

Dynamic NAND

Static NAND

Backgate Coupling Effect
Other Effects

- Capacitive coupling
- Substrate coupling
- Minority charge injection
- Supply noise (ground bounce)
Cascading Dynamic Gates

Only $0 \rightarrow 1$ transitions allowed at inputs!

Domino Logic

Only $0 \rightarrow 1$ transitions allowed at inputs!
**Why Named Domino?**

Like falling dominos!

**Properties of Domino Logic**

- Only non-inverting logic can be implemented
- Very high speed
  - static inverter can be skewed, only L-H transition critical
  - Input capacitance reduced – smaller logical effort
### Domino Logic LE

- \( LE_{A\downarrow} = \)
- \( LE_{i\downarrow} = 1 \)
- \( \bar{\Pi} LE = \)

### Domino Logic LE (skewed static gate)

- Reference inverter:

- \( LE_{A\downarrow} = \)
- \( LE_{i\downarrow} = 1 \)
- \( \bar{\Pi} LE = \)
**Buffer “Average” LE**

Buffer (Domino buffer):

\[ LE_{high} = \frac{2}{3} \]
\[ LE_{low} = \frac{5}{6} \]
\[ \pi LE = \frac{10}{18} \]

“Average” \( LE = \sqrt{10/18} \approx 0.43 \)

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**Designing with Domino Logic**

Diagram of Domino logic gates with PDN (Pass-Transistor Logic Network) and inputs and outputs labeled. The diagram includes transistors labeled as \( M_p \) and \( M_n \), with inputs \( In_1, In_2, In_3 \) and outputs \( Out1, Out2 \). The diagram also notes that the inputs can be eliminated during precharge.

Diagram shows the structure of domino logic gates with labeled components and connections.
Sequential Logic

Output = \( f(\text{In}) \)

Combination vs. Sequential Logic

(a) Combinational

(b) Sequential

Output = \( f(\text{In}, \text{Previous In}) \)
**Why Sequencing?**

Two key (related) reasons that we need sequencing:

1. Want to know when an input has a “new” value

**Why Sequential Logic?**

Two key (related) reasons that we need sequencing:

2. Need to slow down signals that are too fast
   - In order to keep them aligned with slower ones
**Latch versus Register (Flip-flop)**

- **Latch**: level-sensitive
  - clock is low - hold mode
  - clock is high - transparent

- **Register**: edge-triggered
  - stores data when clock rises

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**Characterizing Timing**

- **Register**: $t_{C \to Q}$
- **Latch**: $t_{D \to Q}$
Timing Definitions - REVIEW

![Timing Diagram]

Storage Mechanisms

Static

![Static Storage Mechanism Diagram]

Dynamic

![Dynamic Storage Mechanism Diagram]
Positive Feedback: Bi-Stability

Gain should be larger than 1 in the transition region

Meta-Stability

Gain should be larger than 1 in the transition region
Writing into a Static Latch

Use the clock as a decoupling signal, that distinguishes between the transparent and opaque states

Converting into a MUX

Forcing the state (can implement as NMOS-only)

Pseudo-Static Latch
**Mux-Based Latches**

Negative latch  
(transparent when CLK = 0)

Positive latch  
(transparent when CLK = 1)

\[ Q = \overline{C}_{\text{lk}} \cdot Q + C_{\text{lk}} \cdot \overline{In} \]

\[ Q = \overline{C}_{\text{lk}} \cdot Q + C_{\text{lk}} \cdot In \]

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**Mux-Based Latch**

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**Mux-Based Latch**

- **NMOS only**
- **Non-overlapping clocks**

(a) Schematic diagram

(b) Non-overlapping clocks

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**Latch-Based Design**

- **N latch** is transparent when $\Phi = 0$
- **P latch** is transparent when $\Phi = 1$
Master-Slave (Edge-Triggered) Register

Two opposite latches trigger on edge
Also called master-slave latch pair

Master-Slave Register

Multiplexer-based latch pair
**Clk-Q Delay**

![Diagram showing Clk-Q Delay](image)

**Setup Time**

(a) $T_{setup} = 0.21$ ns

(b) $T_{setup} = 0.20$ ns
More Precise Setup Time

Circuit before clock arrival (Setup-1 case)

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Data $\rightarrow$ Clock $\rightarrow$ T_{Setup-1}

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)