EE141-Spring 2010
Digital Integrated
Circuits

Lecture 9
Transistors

Guest Lecturer:
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Administrativia

- Midterm on Friday Febr 19 6:30-8pm in 2060 Valley LSB
  - Open book
  - Do not forget your important class material nor calculator
  - Covers from start of semester to optimization of complex logic – wires not included!
- Review session tomorrow Th 2/18 at 6:30pm
  - Room to be announced on web-site
- No lab this week
- Hw 4 due next week Friday
Class Material

- Last lecture
  - Wiring + first glimpse at transitors (threshold)
- Today’s lecture
  - Transistor models
- Reading (Ch 3)

MOS Transistor

What do digital IC designers need to know?
With positive gate bias, electrons pulled toward the gate
With large enough bias, enough electrons will be pulled to "invert" the surface (p→n type)
Voltage at which surface inverts: “magic” threshold voltage $V_T$

- Threshold
  \[ V_T = \phi_{FB} + 2\phi_F + \frac{Q_B}{C_{ox}} \]
  \[ V_T = V_{FB} + \gamma \left( \sqrt{2\phi_F + V_{SE}} - \sqrt{2\phi_F} \right) \]

- Fermi potential
  \[ \phi_F = \phi_T \cdot \ln \frac{N_A}{n_i} \]
  $2\Phi_F$ is approximately 0.6V for p-type substrates
  $\gamma$ is the body factor
  $V_{FB}$ is approximately 0.45V for our process
Transistor with Gate and Drain Bias

\[ V_{GS} \quad V_{DS} \]

\[ p\text{-substrate} \]

Transistor in Saturation

\[ 0 < V_{GS} - V_T < V_{DS} \]

\[ V_{DS} > V_{GS} - V_T \]

Pinch-off
Saturation

- For \((V_{GS} - V_T) < V_{DS}\), the effective drain voltage and current saturate:

\[
V_{DS, eff} = (V_{GS} - V_T) \\
I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2
\]

- Of course, real drain current isn’t totally independent of \(V_{DS}\)
  - For example, approx. for channel-length modulation:
    \[
    I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})
    \]

Modes of Operation

Cutoff:
\[V_{GS} - V_T < 0\] \hspace{1cm} I_D = 0

Linear (Resistive):
\[V_{GS} - V_T > V_{DS}\] \hspace{1cm} I_D = \frac{k_n'}{L} \cdot \left[ (V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]

Saturation:
\[0 < V_{GS} - V_T < V_{DS}\] \hspace{1cm} I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})
Current-Voltage Relations: A Good Ol’ Transistor

Current-Voltage Relations: The Deep Sub-Micron Transistor
**Velocity Saturation**

- Velocity saturates due to carrier scattering effects.

\[
\nu_n (\text{m/s})
\]

\[
\xi_c, \xi (\text{V/}\mu\text{m})
\]

\[
\nu_{\text{sat}} = 10^5
\]

Constant velocity

Constant mobility (slope = \(\mu\))

- Velocity saturates due to carrier scattering effects.

**Velocity Saturation**

\[
I_D
\]

\[
V_{GS} = V_{DD}
\]

Long-channel device

Short-channel device

\[
V_{DSAT}, V_{GS} - V_T, V_{DS}
\]
**Including Velocity Saturation**

Approximate velocity:

\[ v = \frac{\mu_n \xi}{1 + \xi / \xi_c} \quad \text{for} \quad \xi \leq \xi_c \]
\[ v = v_{sat} \quad \text{for} \quad \xi \geq \xi_c \]

Continuity requires that:

\[ \xi_c = 2v_{sat}/\mu_n \]

Integrating to find the current again:

\[
I_D = \frac{\mu_n C_{ox} W}{1 + (V_{DS}/\xi_c L)} \left[ \frac{W}{L} \left( V_{GS} - V_T \right)V_{DS} - \frac{V_{DS}^2}{2} \right]
\]
**Regions of Operation**

- Long Channel (L=2.5 \( \mu \)m)
- W/L=1.5
- Short Channel (L=0.25 \( \mu \)m)

**Models, Models, Models...**

- Exact behavior of transistor in velocity sat. somewhat challenging if want simple/easy to use models

- So, many different models developed over the years
  - v-sat, alpha, unified, V_T*, etc.

- Simple model for manual analysis desirable
  - Assume velocity perfectly linear until \( V_{sat} \)
  - Assume \( V_{DSAT} \) constant
**Simplified Velocity Saturation**

- Assume velocity perfectly linear until hit $v_{\text{sat}}$

$$
\begin{align*}
\xi (V/\mu m) & \\
v_n (m/s) & \\
\xi_c = \frac{v_{\text{sat}}}{\mu} & \\
v_{\text{sat}} = 10^5 & \\
\end{align*}
$$

**Simplified Velocity Saturation (cont'd)**

- Assume $V_{\text{DSAT}} = \xi_c L$ when $(V_{GS} - V_T) > \xi_c L$

$$
\begin{align*}
V_{\text{DSAT}} (V) & \\
V_{GS} - V_T (V) & \\
\xi_c L & \\
\xi_c L & \\
\end{align*}
$$
**A Unified Model for Manual Analysis**

Define $V_{GT} = V_{GS} - V_T$

For $V_{GT} \leq 0$: $I_D = 0$

For $V_{GT} \geq 0$:

$$I_D = k\cdot \frac{W}{L} \left(V_{GT} \cdot V_{DS, eff} - \frac{V_{DS, eff}^2}{2}\right) \cdot \left(1 + \lambda \cdot V_{DS}\right)$$

with $V_{DS, eff} = \min(V_{GT}, V_{DS, VSAT})$

**Simplified Model**

- Define $V_{GT} = V_{GS} - V_T$, $V_{D, VSAT} = \xi_c \cdot L$
Simple Model versus SPICE

One Last Simplification

- If device always operates in velocity sat.:
  \[ I_D = k' \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{D,YSAT}}{2} \right) V_{D,YSAT} \]

- "\( V_T^* \)" model:
  \[ V_T^* = V_T + \frac{V_{D,YSAT}}{2} \]
  \[ I_D = k' \frac{W}{L} \left( V_{GS} - V_T^* \right) V_{D,YSAT} \]

- Good for first cut, simple analysis
Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

<table>
<thead>
<tr>
<th></th>
<th>(V_m) (V)</th>
<th>(\gamma) (V(^{0.5}))</th>
<th>(V_{thn}) (V)</th>
<th>(K^*) (A/V(^2))</th>
<th>(\lambda) (V(^{-1}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.43</td>
<td>0.4</td>
<td>0.63</td>
<td>(115 \times 10^{-4})</td>
<td>0.06</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>-0.4</td>
<td>-1</td>
<td>(-30 \times 10^{-4})</td>
<td>-0.1</td>
</tr>
</tbody>
</table>

Textbook: page 103

A PMOS Transistor

- All variables negative
- I prefer to work with absolute values – makes life easier.
MOS Capacitance

\[ C_{GS} = C_{GCS} + C_{GSO} \]

\[ C_{GD} = C_{GCD} + C_{GDO} \]

\[ C_{SB} = C_{diff} \]

\[ C_{GB} = C_{GCB} \]

\[ C_{DB} = C_{diff} \]
Gate Capacitance

- Capacitance (per area) from gate across the oxide is $W \cdot L \cdot C_{ox}$, where $C_{ox} = \varepsilon_{ox} / t_{ox}$

Gate Capacitance

- Distribution between terminals is complex
  - Capacitance is really distributed
    - Useful models lump it to the terminals
  - Several operating regions:
    - Way off, off, transistor linear, transistor saturated
When the transistor is off, no carriers in channel to form the other side of the capacitor.

- Substrate acts as the other capacitor terminal
- Capacitance becomes series combination of gate oxide and depletion capacitance

When $|V_{GS}| < |V_T|$, total $C_{GCB}$ much smaller than $W \cdot L \cdot C_{ox}$

- Usually just approximate with $C_{GCB} = 0$ in this region.

(If $V_{GS}$ is “very” negative (for NMOS), depletion region shrinks and $C_{GCB}$ goes back to $\sim W \cdot L \cdot C_{ox}$)
Transistor in Linear Region

- Channel is formed and acts as the other terminal
  - $C_{GCB}$ drops to zero (shielded by channel)
- Model by splitting oxide cap equally between source and drain
  - Changing either voltage changes the channel charge

Transistor in Saturation Region

- Changing source voltage doesn’t change $V_{GC}$ uniformly
  - E.g. $V_{GC}$ at pinch off point still $V_{TH}$
- Bottom line: $C_{GCS} \approx \frac{2}{3} \cdot W \cdot L \cdot C_{ox}$
Transistor in Saturation Region (cont’d)

- Drain voltage no longer affects channel charge
  - Set by source and \( V_{DS_{sat}} \)

- If change in charge is 0, \( C_{GCD} = 0 \)

Gate Capacitance

\( C_{gate} \) vs. \( V_{GS} \)
(with \( V_{DS} = 0 \))

\( C_{gate} \) vs. operating region
**Gate Overlap Capacitance**

\[ C_O = C_{ox} \cdot x_d \]

Off/Lin/Sat \( \rightarrow \) \( C_{GSO} = C_{GDO} = C_O \cdot W \)

**Gate Fringe Capacitance**

- \( C_{OV} \) not just from metallurgic overlap – get fringing fields too

- Typical value: \(~0.2fF\cdot W\) (in \( \mu m \))/edge