MOSFET Models for Design

- SPICE (BSIM)
  - For verification
  - Device variations

- Hand analysis
  - Velocity-sat model (good mostly for intuition)
  - Small-signal model

- Challenge
  - How to accurately design when hand analysis models may be way off?

Parameters Designers Care About

- Layout designer:
  - Mostly care about just W and L

- Circuit designer:
  - Gain \( g_m \)
  - Bandwidth \( g_m, C_{GS}, C_{GD} \)
  - Power \( I_D \)
  - Voltage swing \( V_{DS} \)
  - Noise

  - Can get many of the circuit parameters without resorting to BSIM
    - Or rather, by just using BSIM as a look-up table

Low Frequency Model

- 1st order Taylor expansion of \( I_D \):
  \[
  i_{ds} = \frac{\partial I_D}{\partial V_{GS}} v_{gs} + \frac{\partial I_D}{\partial V_{DS}} v_{ds} + \frac{\partial I_D}{\partial V_{DS}} v_{ds}
  \]
  \[
  i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + b_{ds} v_{ds}
  \]
  - Just need to know the coefficients...

Square Law Model

- In saturation:
  \[
  g_m = \frac{\mu C_{ox}}{L} \sqrt{\frac{2 I_D}{W}}
  \]
  \[
  g_m = \frac{1}{2} \frac{\mu C_{ox}}{L} I_D \left( V_{GS} - V_P \right)^2 \left( \frac{1}{2} \right) \frac{1}{V_{DS} - V_P}
  \]
  \[
  g_m = 2 \frac{I_D}{V_{GS} - V_T} = \frac{2 I_D}{V_D}
  \]

Weak Inversion \( g_m \)

- In weak inversion we have bipolar behavior
  \[
  I_D \approx \frac{W}{L} I_{DS} \left( e^{\frac{V_{GS} - V_T}{V_P}} - 1 \right)
  \]
  \[
  g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{W}{L} \frac{I_{DS} \left( e^{\frac{V_{GS} - V_T}{V_P}} - 1 \right)}{n e T}
  \]
  - Good model if transistor is actually used in weak inversion
  \[
  g_m = \frac{I_{DS}}{V_D} \approx I_{DS}
  \]
Transconductance

\[ g_m \approx \frac{W}{L} \left( V_{GS} - V_T \right) \]

Weak inversion

Strong inversion

Open-loop Gain \( a_vG \)

- Represents maximum attainable gain from a transistor
  - May be more useful than \( r_o \)

Simulation Notes:
- Bias current \( I_b \) sets \( V_{GS} \) - \( V_T \)
- Use feedback to find correct \( V_{GS} \) while sweeping \( V_{DS} \)
- Use relatively small gain (100) for fast DC convergence

Transconductance (cont)

- Compare \( g_m \) of MOSFET and BJT:
  \[ g_{mFET} = \frac{2I_{ds}}{V_{Vd}} \quad g_{mBJT} = \frac{I_C}{V_t} \]
- Since \( V_{od} \gg V_T \), BJT has larger \( g_m \) for same \( I_o \)

- Why can’t we make \( V_{od} \approx V_T \)?
  - You can – if you work in subthreshold
  - Gives great \( g_m \) per unit current
  - But pay a penalty in speed (will see shortly)

Gain, \( a_vG = g_m r_o \)

Long Channel Gain

\[ L = 0.35 \mu m \]

\[ L \uparrow \rightarrow a_v \uparrow \]

Output Resistance \( r_o \)

Hopeless to model this with a simple equation (e.g. \( g_{ds} = \lambda I_o \))
Technology Trend

Short channel devices usually have lower peak gain.

SPICE Charge Model

- Charge conservation

- MOSFET:
  - 4 terminals: S, G, D, B
  - 4 charges: Q_s + Q_g + Q_d + Q_b = 0 (3 free variables)
  - 3 independent voltages: V_{gs}, V_{ds}, V_{sb}
  - 9 derivatives: C_{ij} = dQ_i / dV_j, e.g., C_{D,G,S} - C_{G,S}
  - C_{ij} != C_{ji}


Small Signal Capacitances

\[
C_{gi} = C_{W,L} \frac{W}{X} \\
C_{iB} = \frac{X}{X} \frac{W}{L}
\]

0.35\mu Process

\[
C_{w,S} = \frac{5.3 \text{ fF/\mu m}^2}{C_{w,G}} = \frac{0.24 \text{ fF/\mu m}}{C_{w,S}} = \frac{0.48 \text{ fF/\mu m}}{C_{w,G}}
\]

Small-Signal AC Model

For practical \( V_{ds} \) gain penalty is less severe (remember: worst case \( V_{ds} \) is what matters!)

Layout

Individual devices:

\[
A_{S} = A_{D} = \frac{1 \mu m}{1} \text{ W} \\
F_{S} = F_{D} = \frac{2 \mu m}{1} \text{ W} \\
e.g., W_{S}, W_{D} = 10 \mu m, \ V_{S}, V_{D} = 0 V \\
C_{S} = 20F \\
C_{D} = 10F
\]

Wide devices consisting of multiple individual ones wired in parallel:

\[
A_{S} = A_{D} = \frac{1 \mu m}{1} \text{ W} \\
F_{S} = F_{D} = \frac{2 \mu m}{1} \text{ W} \\
e.g., W_{S}, W_{D} = 20 \mu m, \ V_{S}, V_{D} = 0 V \\
C_{S} = 20F \\
C_{D} = 10F
\]
**Source/drain Parasitics and HSPICE**

- ACM = 3 model (not in our current library)
  - HDIF = half of heavily doped diffusion length
- GEO = 0: No sharing
- GEO = 1: Drain shared
- GEO = 2: Source shared
- GEO = 3: Both shared

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**Efficiency as a Design Parameter**

- Why not use \( g_m / I_D \) for design?
- Can always determine value (from \( I_D \) and \( g_m \))
  - Can do this “independently” of short channel effects (using simulator)
- Units (\( V^{-1} \)) and physical interpretation a little strange
  - But we’ll just redefine things slightly to fix this

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**Figure of Merit: \( g_m / I_D \)**

\[
g_m = \frac{1}{\sqrt{4kT}} \quad \text{and} \quad \frac{g_m}{I_D} = \frac{2}{V_{gs} - V_T} = \frac{2}{V_{dsat}}
\]

- How much \( g_m \) per unit current
- Purely a DC metric
  - Weak and moderate inversion region clearly the most efficient regions to operate in

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**Substitute for \( g_m / I_D \): \( V^* \)**

- Define:
  \[
  V^* = \frac{2I_D}{g_m} \quad \Rightarrow \quad \frac{g_m}{I_D} = \frac{2}{V^*}
  \]
- Square-law devices: \( V^* = V_{gs} - V_{th} = V_{sd} \)
- Remember: real devices do not obey the square law!

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**Efficiency \( g_m / I_D \)**

- In weak or moderate inversion, approaches BJT
  \[
  g_m / I_c = 1 / V_i \approx 40 \, V^{-1}
  \]
- Largely independent of device type
  - NMOS/PMOS about the same

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**Dynamic Figure of Merit**

- Unity current-gain bandwidth
  \[
  \omega_T = \frac{g_m}{C_{gs} + C_{gd}}
  \]
  \[
  \omega_T = \frac{3 \mu V_{dsat}}{2 I_c} \quad \text{(Long channel model, } C_{gd}=0)\]
- For degenerate short channel device
  \[
  \omega_T = \frac{3 \mu V_{real}}{2 I_c} \quad \text{for } \frac{1}{2} r_{osat}
  \]
**Efficiency $g_m/I_D$ versus $f_T$**

- NMOS faster than PMOS
- Speed-Efficiency Tradeoff
- 0.35 µm Process

**$V_{od}$ vs $V^*$**

- Overdrive voltage $V_{od}$
  - Cannot be measured
  - Complex equations
- "Long channel" devices:
  - $V_{od} = V_{dsat} = V^*$
  - $I_D \propto V^2$
  - Boundary between triode and saturation
  - $f_T$ "large" for $V_{dsat} > V^*$
  - $C_{GS}, C_{GD}$ change
- "Short channel" devices:
  - All interpretations of $V^*$ are approximations
  - Except $V^* = 2I_D/g_m$ (but $V^* \neq V_{dsat}$)

**Device Scaling**

- Short channel devices significantly faster

**Composite Figure-of-Merit: $f_T \cdot g_m/I_D$**

- Peak performance for low $V_{dsat} - V_{th}$ (implies low $V^*$)

**Design Example**

- Example: Common-source amp $a_u > 70, f_u = 100$ MHz for $C_L = 5$ pF
  - $a_u > 70 \Rightarrow L = 0.35 \mu m$
  - $g_m = 2\pi \cdot C_L = 3.14 \text{ mS}$
  - High $f_t$ (small $C_{gd}$): $V^* = 200 \text{ mV}$
  - $I_D = \frac{V^*}{2} = 314 \mu A$

**Device Sizing**

- Pick $L = 0.35 \mu m$
- Pick $V^* = 200 \text{ mV}$
- Determine $g_m = 3.14 \text{ mS}$
- $I_D = 0.5 \cdot g_m \cdot V^* = 314 \mu A$
- $W$ from graph (generate with SPICE)
  - $W = 10 \mu m (314 \mu A / 141 \mu A) = 22 \mu m$
- Create these graphs for several device lengths
Common Source Verification

- Amplifier gain > 70
- Amplifier unity gain frequency is "dead on"
- Output range limited to 0.6 V – 1.5 V to maintain gain (about ±0.45V swing)

Small Signal Design Summary

- Determine $g_m$ (from design objectives)
- Pick L
  - Short channel $\rightarrow$ high $f_T$
  - Long channel $\rightarrow$ high $r_o$, $a_v$, better matching
- Pick $V^*$ = $2L/g_m$ based on qualitative interpretation
  - Small $V^*$ $\rightarrow$ large signal swing, high current efficiency
  - High $V^*$ $\rightarrow$ high $f_T$
  - Also affects noise (see later)
- Determine $I_D$ (from $g_m$ and $V^*$)
- Determine W (SPICE / plot) $\leftarrow$ takes care of short channel effects, etc.
- Accurate for short channel devices $\rightarrow$ key for design

Device Parameter Summary

<table>
<thead>
<tr>
<th>Device Parameter</th>
<th>Circuit Implications</th>
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| $V^*$            | Current efficiency, $g_m/I_D$  
|                  | Power dissipation ($I_D$)  
|                  | Speed ($g_m$)  
|                  | Cutoff frequency, $f_T$ $\rightarrow$ phase margin, noise  
|                  | Headroom, $V_{DS,MIN}$  
| $L$              | Cutoff frequency, $f_T$ $\rightarrow$ phase margin, noise  
|                  | Intrinsic transistor gain ($a_v$)  
| $W$              | Obtain from $L$, $I_D$ (complicated equations!)  
|                  | Self loading ($C_{GSS}$, $C_{GDS}$, ...)  

Device Sizing Chart

Generate these curves for a variety of L’s and device flavors (NMOS, PMOS, thin oxide, thick oxide, different $V_{TH}$)