Comparator

- Specs and issues:
  - Clock rate $f_s$
  - Offset
  - Resolution
  - Hysteresis
  - Input cap
  - Power dissipation
  - CM rejection
  - Kickback noise
  - ...

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Flash Converter

- Fast: one clock cycle per conversion
- High complexity: $2^B - 1$ comparators
- High input capacitance

Comparator Gain-Bandwidth

**Example:**

- 4Gb/s link
- Minimum $\Delta V$: 1mV
- $V_{dd} = 1V$

$A_v > \frac{1V}{1mV} = 1000 \text{ in } < 250\text{ps}$!
Operational Amplifier?

\[ f_{-3dB} = \frac{f_u}{A_{in}} = \frac{2}{3} \frac{1}{T_{bit}} \]

\[ f_u = \frac{2A_{in}}{3T_{bit}} = \frac{1000}{3 \times 250 \text{ps}} = 1.33 \text{THz} \]

Open-Loop Amplifier Cascade
Cascaded Amplifier

• Simplified bandwidth analysis:
  • Open-circuit time constants
  • (Not most accurate, but leads to nearly the right answer for design optimization)

Bandwidth/Gain Optimization
Bandwidth/Gain Optimization

Power Consumption
Regenerative Latch

CML Comparator (Latch)
StrongArm Latch

Another CMOS Comparator
Hysteresis

Kickback
Kickback cont’d