Offset

• To achieve zero offset, comparator devices must be perfectly matched to each other
• How well-matched can the devices be made?
  • Not arbitrary – direct function of design choices

Sources of Local Variation

• Deterministic sources:
  • Local poly density
  • Sub-90nm: stress, litho interactions, ...

• Random sources:
  • Dopant fluctuations
  • Line-edge roughness
  • Oxide traps

• Focus our modeling on random variations
  • Deterministic handled with good layout practices

Device Mismatch Categories

• Die-to-die
  • All devices on same chip (or wafer) have same characteristics

• Within die (long-range)
  • All devices within certain region have same characteristics

• Local (short-range)
  • Every device different, random
  • Usually most important source of mismatch

References

  • Mismatch model
  • Statistical data for 2.5µm CMOS

  • 0.18µm CMOS data

Mismatch Statistics

• Total mismatch set by composite of many single, independent events
  • Correlation distance << device dimensions
  • E.g., number of dopant atoms implanted into the channel

• Individual effects are small: linear superposition holds

•Mismatch is zero mean, Gaussian distribution
Parameter Mismatch Model

\[ \sigma^2(\Delta P) = \frac{\sigma_P^2}{WL} + S_P^2 D_t^2 \]

\( \sigma^2(\Delta P) \): standard deviation of \( P \)
\( WL \): active gate area
\( D_t \): distance between device centers
\( A_P \): measured area proportionality constant
\( S_P \): measured distance proportionality constant,
\( : \neq 0 \) for "good" layout

V_T Mismatch

- Mismatch in \( V_T \) between two identical devices:

\[ \sigma^2 (\Delta V_T) = \frac{A_{V_T,MAX}}{WL} + S_{V_T} D_t^2 \]

2.5\( \mu \)m CMOS process:
\( A_{V_T,MAX} \approx 30 \text{ mV/\mu m} \)
\( A_{V_T,MIN} \approx 35 \text{ mV/\mu m} \)

- Often largest source of offset

Back-Gate Bias, \( V_{SB} \)

- Mismatch can depend on \( V_{SB} \)

- Why?

Current Matching, \( \Delta I_D/I_D \)

Strong bias dependence (we knew that already)

Drain Bias, \( V_{DS} \)

\( \Delta V_T \) largely independent of \( V_{DS} \)

Current Factor

\[ \beta = \mu C_{ox} \frac{W}{L} \]
Sources of $\beta$ Mismatch

- Mobility variations
  - E.g., due to dopant variations, random defects
- Oxide thickness variation
  - Usually very well-controlled
- Edge roughness

Distance Effect

Process Dependence

- $A_{ox}$ tends to scale with technology
- Proportional to $t_{ox}$
- Also depends on doping level

Orientation Effects

- Si and transistors are not (perfectly) isotropic
- $\rightarrow$ keep direction of current flow same!

0.18 $\mu$m CMOS
Current Matching

Voltage Matching

“Golden Rule” of Layout for Matching

- Everything you can think of might matter
- Even whether or not there is metal above the devices
- How to avoid systematic errors?


Common Centroid Layout

- Cancels linear gradients
- Required for moderate matching

Simulating Mismatch

- Brute force: Monte Carlo
- HSPICE “throws the dice”...