EECS240 – Spring 2009

Lecture 2: CMOS Technology and Passive Devices

Elad Alon
Dept. of EECS

Today’s Lecture

• EE240 CMOS Technology

• Passive devices
  • Motivation
  • Resistors
  • Capacitors
  • (Inductors)

• Next time: MOS transistor modeling

Process Options

• Available for many processes

• Add features to “baseline process”

• E.g.
  • Silicide block option
  • “High voltage” devices (2.5V & 3.3V, >10V)
  • Low $V_{th}$ devices
  • Capacitor option (2 level poly, MIM)
  • …

EE240 Process

• 90nm 1P7M CMOS
  • Minimum channel length: 90nm
  • 1 level of polysilicon
  • 7 levels of metal (Cu)
  • 1.2V supply
  • Models for this process not “real”

• Other processes you might see
  • Shorter channel length (45nm / 1V)
  • Bipolar, SiGe HBT
  • SOI

Dimensions

CMOS Cross Section

Drawing is not to scale!
Why Talk About Passives?

Resistors

- No provisions in standard CMOS
- Resistors are bad for digital circuits →
  - Minimized in standard CMOS
  - But, often want big, well-controlled R for analog...
- Sheet resistance of available layers:

<table>
<thead>
<tr>
<th>Layer</th>
<th>Sheet resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>60 mΩ/□</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>5 Ω/□</td>
</tr>
<tr>
<td>N+/P+ diffusion</td>
<td>5 Ω/□</td>
</tr>
<tr>
<td>N-well</td>
<td>1 kΩ/□</td>
</tr>
</tbody>
</table>

Silicide Block Option

<table>
<thead>
<tr>
<th>Layer</th>
<th>$R(T)$ [Ω/□]</th>
<th>$T_C$ [ppm/°C] @ $T = 25$ °C</th>
<th>$V_C$ [ppm/V]</th>
<th>$B_C$ [ppm/V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>N+ poly</td>
<td>100</td>
<td>-800</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>P+ poly</td>
<td>180</td>
<td>200</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>N+ diffusion</td>
<td>50</td>
<td>1500</td>
<td>500</td>
<td>-500</td>
</tr>
<tr>
<td>P+ diffusion</td>
<td>100</td>
<td>1600</td>
<td>500</td>
<td>-500</td>
</tr>
<tr>
<td>N-well</td>
<td>1000</td>
<td>-1500</td>
<td>20,000</td>
<td>30,000</td>
</tr>
</tbody>
</table>

- Non-silicided layers have significantly larger sheet resistance
- Resistor nonidealities:
  - Temperature coefficient: $R = f(T)$
  - Voltage coefficient: $R = f(V)$
- Manufacturing Variations

Resistor Example

Goal: $R = 100$ kΩ. $T_C = 1/R \times dR/dT = 0$

Example Solution: N+ and P+ poly resistors in series

$$R = R_1(1 + T_C \Delta T) + R_2(1 + T_C \Delta T) = R_1 + R_2 + (R_1 T_C + R_2 T_C) \Delta T \Rightarrow R_C = R_1 \frac{1}{1 + \frac{T_C}{T_{C1}}} = 20\,\text{kΩ} = 200\,\text{squares}$$

$$R_C = R_1 \frac{1}{1 + \frac{T_C}{T_{C2}}} = 80\,\text{kΩ} = 444.4\,\text{squares}$$

Voltage Dependence
Voltage Coefficient

Example:
Diffusion resistor
\[ R = \frac{V_2 - V_1}{I} = R \left[ 1 + \frac{z_f}{2} + \frac{1}{V_T} + 2 \frac{1}{V_T} \right] \]

Applied voltage modulates depletion width (cross-section of conductive channel)

Well acts as a shield

Resistor Matching

- Types of mismatch:
  - Run-to-run variations
  - Global differences in thickness, doping, etc.
  - Systematic (e.g., contacts)
  - Random variations between devices

- Run-to-run variations in absolute R value: 20+%
  - Can be problematic for termination, bias current, etc.

- Best case: make circuit depend only on ratios
  - E.g., use feedback to control opamp gain
  - With careful layout, can get 0.1 – 1% matching

Resistor Layout (cont.)

Serpentine layout for large values:

Better layout (mitigates offset due to thermoelectric effects):


Systematic Variations from Layout

- Example:
  - \[ R = \frac{V_1}{I} \]

- 2R?

- Use unit element instead:
  - \[ 2R \]

MOSFETs as Resistors

- Triode region (“square law”):
  \[ I_D = \mu C_w \frac{W}{L} \left( V_{DS} - V_t - \frac{V_{GS}}{2} \right)^2 \]
  - For \( V_{GS} > V_T \)

- Small signal resistance:
  \[ R = \frac{1}{\frac{\partial I_D}{\partial V_{GS}}} \]
  \[ R = \frac{1}{\mu C_w \frac{W}{L} \left( V_{GS} - V_T \right)} \]
  - For \( V_{GS} - V_T >> V_T \)

- Voltage coefficient:
  \[ V_{DS} \frac{1}{R} \]
  \[ V_{GS} \]
  \[ 1 \]
  \[ V_{DS} - V_{GS} \]
MOS Resistors

**Example:**
\[ R = \frac{1}{\mu C (V_{GS} - V_{TH})} \]
- Large R-values realizable in small area
- Very large voltage coefficient

**Applications:**
- MOSFET-C filters: (linearization)
- Biasing: (>1 GΩ)

Resistor Summary
- No or limited support in standard CMOS
  - Large area (compared to FETs)
- Nonidealities:
  - Large run-to-run variations
  - Temperature coefficient
  - Voltage coefficients (nonlinear)
- Avoid them when you can
  - Especially in critical areas, e.g.
    - Amplifier feedback networks
    - Electronic filters
    - A/D converters
- We will get back to this point

Capacitors
- “Improved” capacitor:

\[ \frac{1}{1 + \frac{1}{2V}} = 0.95 \, \text{V}^{-1} \]

Capacitor Options

<table>
<thead>
<tr>
<th>Type</th>
<th>( C ) [aF/µm²]</th>
<th>( V_C ) [ppm/V]</th>
<th>( T_C ) [ppm/°C]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate</td>
<td>10,000</td>
<td>Huge</td>
<td>Big</td>
</tr>
<tr>
<td>Poly-poly (option)</td>
<td>1000</td>
<td>10</td>
<td>25</td>
</tr>
<tr>
<td>Metal-metal</td>
<td>50</td>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td>Metal-substrate</td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal-poly</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Poly-substrate</td>
<td>120</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction caps</td>
<td>~ 1000</td>
<td>Big</td>
<td>Big</td>
</tr>
</tbody>
</table>

Capacitors
- Simplest capacitor:

\[ \text{substrate} \]

What’s the problem with this?

MOS Capacitor
- High capacitance in inversion

\[ C = \frac{I}{V} \]
- SPICE:
  \[ V = 0 \rightarrow C = I \]
MOS Capacitor

- High non-linearity, temperature coefficient
- But, still useful in many applications, e.g.:
  - (Miller) compensation capacitor
  - Bypass capacitor (supply, bias)

Capacitor Geometries

- Horizontal parallel plate
- Vertical parallel plate
- Combinations


Capacitor Layout

- Unit elements
- Shields:
  - Etching
  - Fringing fields
  - "Common-centroid"
- Wiring and interconnect parasitics


MIM Capacitors

- Some processes have MIM cap as add-on option
  - Separation between metals is much thinner
  - Higher density
- Used to be fairly popular
  - But not as popular now that have many metal layers anyways

“MOM” Capacitors

- Metal-Oxide-Metal capacitor. Free with modern CMOS.
- Use lateral flux (\( \Phi_{\text{lateral}} \)) and multiple metal layers to realize high capacitance values


MOM Capacitor Cross Section

- Use a wall of metal and vias to realize high density
- More layers – higher density
  - May want to chop off lower layers to reduce capacitance
- Reasonably good matching and accuracy
Distributed Effects

- Can model IC resistors as distributed RC circuits.
- Could use transmission line analysis to find equivalent 2-port parameters.
- Inductance negligible for small IC structures up to ~10GHz.

\[ R \gg \omega L \]

Effective Resistance

- High frequency resistance depends on \( W \), e.g.:
  - \( W=1 \mu \) 10k\( \Omega \) resistor works fine at 1GHz
  - \( W=5 \mu \) 10k\( \Omega \) resistor drops to 5k\( \Omega \) at 1 GHz
- May need distributed model for accurate freq response

Double Contact Structure

- If contact on both edges,
  - \( R \) drops 4X
  - Can be a good idea even if not hitting distributed effects

Capacitor Q

- Current density drops as you go farther from contact edge...

What About Inductors?

- Mostly not used in analog/mixed-signal design
- Usually too big
- More of a pain to model than R’s and C’s
- But they do occasionally get used
- Example inductor app.: shunt peaking
  - Can boost bandwidth by up to 85%
  - Q not that important (L in series with R)
  - But frequency response may not be flat

Spiral Inductors

- Used widely in RF circuits for small L (~1-10nH).
- Use top metal for Q and high self resonance frequencies.
  - Very good matching and accuracy – if you model them right