EE241 - Spring 2000
Advanced Digital Integrated Circuits

Lecture 5
Circuit Optimization for Speed
High-Speed Logic Families

Announcements

- Tu 2/8/00 class will be pre-taped on Friday, 2/4, 4-5:30pm; will be replayed in normal lecture time; and will be available for review on tape
- Th 2/10/00 class will start 10 mins early – exactly at 2pm
- Projects – proposals due 2/8/00 by 5pm
- Send me an e-mail containing – names, title and URL
- Homework #1 will be posted on Friday, due in 2 wks
- ISSCC preview seminars:
  » Thu 2/3 4-5 531 Cory – 2 speakers from UC Davis (analog)
Differential Logic

- Differential Cascode Voltage Switch (DCVS)
- Differential Split-Level (DSL)
- Cascode Non-Threshold Logic (CNTL)
- Regenerative Push-Pull Cascode Logic (PPCL)
- Pass transistor logic families
- Dynamic logic families

Cascode Voltage Switch Logic

Sometimes called Differential Cascode Voltage Switch Logic (DCVSL)

Heller
ISSCC'84
CVSL

Fast
No static power dissipation

Full adder design

How to design for reduced transistor count?
Karnaugh Map Technique

Example: $Q = x_1 x_2 + x_3 x_0 + x_2 x_1$

Connect "0" tree to $\bar{Q}$
"1" tree to $Q$

Chu, Pulfrey
JSSC12/86
Example

\[ Q = x_1x_2x_3x_4 + x_1(x_2 + x_3 + x_4) \]

Using Ordered BDDs

Example: 
\[ f = x_1x_2 + x_1x_3 + x_1x_4 \]
\[ = x_1(x_2 + x_3) + x_1(x_2x_3) \]
Push-Pull Cascode Logic


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DSL - Differential Split-Level Logic

Reduce swing at nodes $Q$ and $\overline{Q}$ to, say, $V_{DD}/2$

$V_{REF} = V_{DD}/2 + V_{TH}$

Pfennings et al, JSSC 10/85

Smaller DS voltage on PDN transistors
Smaller field, no hot electron effects
Comparison of CMOS Circuit Techniques

CVSL trees:

Conv. CMOS trees:
### Simulation Results for Different Adders

<table>
<thead>
<tr>
<th>CIRCUIT TECHNIQUE</th>
<th>INPUT RISE CAPACITANCE (pF)</th>
<th>OUTPUT LOAD CAPACITANCE (pF)</th>
<th># OF P-DES</th>
<th># OF N-DES</th>
<th>WORST CASE DELAY TIME (ns)</th>
<th>AVERAGE POWER DENSITY AT 50 MHz (mW)</th>
<th>NORMALIZED POWER-DELAY PRODUCT</th>
</tr>
</thead>
<tbody>
<tr>
<td>STATIC FULL CMOS</td>
<td>155</td>
<td>155</td>
<td>15/15</td>
<td>20</td>
<td>0.58</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>STATIC DCVS</td>
<td>85</td>
<td>85</td>
<td>4/18</td>
<td>22</td>
<td>1.11</td>
<td>2.11</td>
<td>2.11</td>
</tr>
<tr>
<td>STATIC CSL</td>
<td>85</td>
<td>85</td>
<td>4/22</td>
<td>14</td>
<td>1.25</td>
<td>1.63</td>
<td>1.63</td>
</tr>
<tr>
<td>NORMA</td>
<td>110</td>
<td>220</td>
<td>12/10</td>
<td>18</td>
<td>0.83</td>
<td>1.29</td>
<td>1.29</td>
</tr>
<tr>
<td>MODIFIED NORMA</td>
<td>45</td>
<td>90</td>
<td>8/20</td>
<td>10</td>
<td>1.24</td>
<td>1.06</td>
<td>1.06</td>
</tr>
<tr>
<td>DCVS NORMA</td>
<td>85</td>
<td>170</td>
<td>12/20</td>
<td>10</td>
<td>1.55</td>
<td>1.34</td>
<td>1.34</td>
</tr>
<tr>
<td>DCVS D3KND</td>
<td>85</td>
<td>170</td>
<td>12/24</td>
<td>9</td>
<td>1.75</td>
<td>1.36</td>
<td>1.36</td>
</tr>
</tbody>
</table>


### Cascode Non-Threshold Logic

No reference voltage $V_{REF}$

Performance? Capacitors?

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Cascode Non-Threshold Logic

Can an inverter be used as an amplifier?

Can an amplifier be used as an inverter?

CVSL Properties

- Static
- No static power, except DSL leakage
- Process and supply tolerance is an issue with DSL
Pass-Transistor Logic Styles

- Static Pass-Transistor Logic
  - Transmission gates
  - Complementary PTL (CPL)
  - Dual (DPL)
  - Reduced DPL (DVL)
  - Swing restoration techniques – SRPL, SAPL, DCVSPG

Pass-Transistor Logic

- N transistors
- No static consumption
- Transistor implementation using NMOS
NMOS-only switch

$V_B$ does not pull up to 2.5V, but $2.5 - V_{TN}$

Threshold voltage loss causes static power consumption

NMOS-Only Switch

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Pass-Transistor Logic Families

<table>
<thead>
<tr>
<th>Logic Load</th>
<th>NMOS Logic</th>
<th>Pass-Transistor Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS Cross-Coupled</td>
<td>CVSL (IBM, 1984)</td>
<td>DCVSPG (IBM, 1993)</td>
</tr>
<tr>
<td>CMOS Inverter</td>
<td>DSL (Philips, 1985)</td>
<td>CPL (Hitachi, 1990)</td>
</tr>
<tr>
<td>None</td>
<td>DPL (Hitachi, 1993)</td>
<td>SRPL (Toshiba, 1994)</td>
</tr>
<tr>
<td>CMOS Latch</td>
<td></td>
<td>SAPL (Toshiba, 1994)</td>
</tr>
<tr>
<td>Sense Amplifier</td>
<td></td>
<td></td>
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</tbody>
</table>

Pass-Transistor Logic Families

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Complementary Pass-Transistor Logic (CPL)

- Complementary functions
- Reduced number of logic levels
- Much less transistors than CMOS
- Fast – reduced load
- Complementary inputs – complementary outputs
- $V_T$ drop – several solutions

CPL

Yano et al, JSSC CICC’89, 4/90
CPL

Same topology of networks
Just different signal arrangements

Complementary Pass-Transistor Logic (CPL)

nFET logic network
- Fast
- $V_T$ drop
- Efficient implementation of arithmetic

XOR

Sum
CPL

Yano – CICC’89: 0.5µm CMOS with dual thresholds

\[ V_{DD} \]
\[ V_{DD} \]
\[ V_{DD} \]
\[ 0V \]
\[ 5V \]
\[ 5V \]
\[ V_{DD} \]
\[ V_{DD} \]
\[ V_{DD} \]
\[ V_{Th} = 0V \]
\[ V_{Th} = 0.4V \]
\[ 0V \]
\[ 5V \]
\[ 0V \]
\[ Out \]

WATCH OUT FOR LEAKAGE CURRENTS

CPL vs. CMOS

<table>
<thead>
<tr>
<th>Transistor Count</th>
<th>CMOS</th>
<th>CPL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>4710µm²</td>
<td>4218 µm²</td>
</tr>
<tr>
<td>Delay (4V)</td>
<td>0.63ns</td>
<td>0.26ns</td>
</tr>
<tr>
<td>Power (100MHz)</td>
<td>1.2mW</td>
<td>0.65mW</td>
</tr>
</tbody>
</table>

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Skewing Output Inverter

CPL vs. CMOS
Differential vs. Single-Ended

<table>
<thead>
<tr>
<th>CLA Circuit</th>
<th>Single-Ended Pass Transistor Logic</th>
<th>CPL</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>![Single-Ended Pass Transistor Logic Diagram]</td>
<td>![CPL Diagram]</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>82</td>
<td>86</td>
</tr>
<tr>
<td>Delay (C₀-C₉)</td>
<td>0.26ns</td>
<td>0.15ns</td>
</tr>
</tbody>
</table>

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CPL Performance

- Implemented 16 x 16bit multiplier
- 3.8ns (@ 300K) in 0.5µm CMOS
- Wallace tree + CLA in final adder

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CPL vs. Supply Voltage

Impact of Vdd on Pass Transistor Fan-Inverter

Level Restoring

Level Restorer

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Level Restoring

Different level restoration leads to different logic families

Single-Ended Level Restoring

Feedback Inverter

Output Inverter

Level Restoration Transistor
Lean Cell Library

Yano et al, CICC’94, JSSC 6/96

Various Logic Functions of the Lean Library

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Yano et al, CICC’94, JSSC 6/96

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### LEAP Comparison

**3 input CMOS NAND**
6 Xtrs, 329\(\mu\)m\(^2\), 295pS, 0.91\(\mu\)W/MHz

**3 input Y2 NAND**
13 xtrs, 579\(\mu\)m\(^2\), 465pS, 0.96\(\mu\)W/MHz

**Overall 3 input functions**

<table>
<thead>
<tr>
<th></th>
<th>3 input MUX</th>
<th>3 input NAND</th>
</tr>
</thead>
<tbody>
<tr>
<td>avg cell #</td>
<td>1.92</td>
<td>3.09</td>
</tr>
<tr>
<td>avg input connections</td>
<td>5.11</td>
<td>11.4</td>
</tr>
<tr>
<td>avg cascade depth</td>
<td>2.23</td>
<td>3.08</td>
</tr>
</tbody>
</table>

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### Leap Comparison

**Summary of the Comparison Results of Cells**

<table>
<thead>
<tr>
<th></th>
<th>4-b Adder/Subtractor</th>
<th>7-in, 4-Out Random Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CMOS</td>
<td>LEAP</td>
</tr>
<tr>
<td>Tr. Count /Cell</td>
<td>6.22</td>
<td>6.41</td>
</tr>
<tr>
<td>Gate Width / Cell</td>
<td>57(\mu)m</td>
<td>36(\mu)m</td>
</tr>
<tr>
<td>Net Count / Cell</td>
<td>2.9</td>
<td>4.7</td>
</tr>
<tr>
<td>Area / Cell</td>
<td>635(\mu)m(^2)</td>
<td>571(\mu)m(^2)</td>
</tr>
<tr>
<td>Delay Time / Cell</td>
<td>0.302ns</td>
<td>0.269ns</td>
</tr>
<tr>
<td>Power / Cell</td>
<td>45.7(\mu)W/MHz</td>
<td>45.2(\mu)W/MHz</td>
</tr>
</tbody>
</table>
LEAP Performance

Supply Voltage $V_C$ (V) vs. Threshold Voltage $V_{th}$ (V)

- LEAP faster than CMOS
- $V_C = 2.7V_{th}$

Delay Time (ns) vs. Supply Voltage (V)

4-bit ADD-SUB

$V_{th} = 0.67V$

CMOS vs. LEAP