EE241 - Spring 2000
Advanced Digital Integrated Circuits

Lecture 7
Pass-Transistor Logic Families

Announcements

- This lecture is being replayed in normal lecture time; and will be available for review on tape
- Th 2/10/00 class will start exactly at 2pm
- Projects – proposals due 2/10/00 by 5pm
- Homework #1 will be posted on Friday evening
Different Restoration Schemes

Swing-Restored Pass-Transistor Logic

Swing-Restored Pass-Transistor Logic

Parameswar, et al
CICC'94, JSSC 6/96
Swing-Restored Pass-Transistor Logic

Full adder

Worst case delays
Swing-Restored Pass-Transistor Logic

**Comparison of Full Adder Circuits**

<table>
<thead>
<tr>
<th></th>
<th>CMOS</th>
<th>CPL</th>
<th>DPL</th>
<th>DCVS PG</th>
<th>SRPL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed (ns)</td>
<td>0.82</td>
<td>0.44</td>
<td>0.63</td>
<td>0.53</td>
<td>0.44</td>
</tr>
<tr>
<td>Power at 100MHz (mW)</td>
<td>0.52</td>
<td>0.42</td>
<td>0.58</td>
<td>0.3</td>
<td>0.19</td>
</tr>
<tr>
<td>Power-Delay Product (normalized)</td>
<td>1.0</td>
<td>0.43</td>
<td>0.86</td>
<td>0.37</td>
<td>0.21</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>40</td>
<td>28</td>
<td>48</td>
<td>24</td>
<td>28</td>
</tr>
</tbody>
</table>

Parameswar, JSSC 6/96

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Other Level-Restoring Schemes

a) CPL  

b) SRPL  

UC Berkeley EE241  B. Nikolic
Other Level-Restoring Schemes

Energy Economized Pass-Transistor Logic

DCVS with Pass Gates (DCVS-PG)

DCVSPG

UC Berkeley EE241 B. Nikolic