This is an individual assignment!

1. **Conditional sum adder**
   a) Find an error in a table that demonstrates conditional sum addition in slide 24, of lecture 18 notes.
   b) Demonstrate the conditional summation by a similar table for inputs \( x = 10110110 \) and \( y = 01001101 \).

2. **Ling adder**
   Read the article “A sub-nanosecond 0.5\( \mu \)m 64-bit adder design,” by S. Naffziger presented at 1996 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 362-363.
   a) Reconstruct the key logic equations (from the inputs to the outputs) in the design of this adder.
   b) Draw the parallel prefix tree that this adder implements.

3. **Sparse Ling adder**
   Draw the sum precompute gates for a sparse 64-bit Ling adder with a sparseness of 2. The final sum for both odd and even bits should be performed by selecting one of the possible precomputed sums using the available carry. Use domino logic.