EE241 - Spring 2003
Advanced Digital Integrated Circuits

Lecture 26
High-Speed Links
Guest Lecturer: Jared Zerbe, Rambus Inc.

Agenda: High Speed Links

- Background
- The Problem
- Key components
- Results
- Future areas
Background: Where Links?

- Chip-2-Chip
- Cables
- Single connector
- Backplanes

Increasing complexity

What Makes a Link?

- Signaling: sending and receiving the information
- Clocking: Determining which bit is which
Spanning A Broad Space

- Inverter.........to........DSL modem
- Metrics
  - Speed
  - Latency
  - Electrical environment
  - Power & area
  - Volume

Serial Link Signaling Over Backplanes

- Very challenging signaling environment
  - Almost no signal left at receiver
The Backplane Environment

- The problem is there are many sources of $Z$ …and thus many possible sources of reflections

SI drives Si above 3Gb/s

- We must understand much more about the problem to operate above 3Gb/s
Key Problems In The Backplane

- Background
- The Problem
  - Loss
  - Reflections
  - Crosstalk
  - Skew
- Key components
- Results
- Future areas

Problems: Material Loss

- PCB Loss: skin & dielectric loss
  - Skin Loss $\propto \sqrt{f}$
  - Dielectric loss $\propto f$: a bigger issue at higher $f$
Problems: Reflections

Sources of Reflections: Z - Discontinuities

- PCB Z mismatch
- Connector Z mismatch
- Vias (through) Z mismatch
- Device parasitics - effective Z mismatch

\[
\begin{align*}
Z_1 & \quad \text{via} \quad \text{Conn} \quad \text{via} \quad \text{BP} \\
\text{Energy flow into junction} & = \text{transmitted} + \text{reflected energy}
\end{align*}
\]

Discontinuities + Energy \( @ F \) = Resonance

Roger BP, Length: 1.5", T/S: 29/264 mil

Resonant notch due to via stub
Reflections From Via Stubs

- Additional sources of reflections: stubs
  - Vias - particularly on thick backplanes
  - Package plating stubs

Signaling With Stubs: DRAM example
Shortening Stubs & Tuning Z

Problems: Crosstalk

- Many sources
  - On-chip
  - Package
  - PCB traces
  - Inside connector

- Differential signaling can help
  - Minimize crosstalk generation & make effects common-mode

- Both NEXT & FEXT
  - NEXT very destructive if RX and TX pairs are adjacent
    - Full swing-TX coupling into attenuated RX signal
    - Effect on SNR is multiplied by signal loss
  - Simple solution: group RX/TX pairs in connector
  - NEXT typically 3-6%, FEXT typically 1-3%
Problems: Skew

- A router can have
  » 1,000’s, even 10,000’s of links
  » Sources from any linecard to any switch-card port
  » Clocking and delay matching is a nightmare!

- Matching skew across all switch card inputs would make backplane routing impossible
  » Make each link independent and use CDR
    - Don’t need to worry about clock or data skews across BP
  » Still need to match skews within differential pair
    - Otherwise can have modal conversion loss & EMI problems

A Complex System

![Diagram showing frequency response](image-url)
Key Components In Links

- Background
- The Problem
- Key components
  - Loss: Equalization, MLS
  - Reflections: Termination, active methods
  - Skew: Clocking and PLLs, CDRs
  - TX & RX Design
- Results
- Future areas

Equalization For Loss:
Goal is to Flatten Response

- Channel is band-limited
- Equalization: boost high-frequencies relative to lower frequencies
Receive Linear Equalizer

- Amplifies high-frequencies attenuated by the channel
- Pre-decision
- Digital or Analog FIR filter
- Issues
  - Also amplifies noise!
  - Precision
  - Tuning delays (if analog)
  - Setting coefficients
    - Adaptive algorithms such as LMS

Transmit Linear Equalizer

- Attenuates low-frequencies
  - Need to be careful about output amplitude: limited output power
    - If you could make bigger swings, you would
    - EQ really attenuates low-frequencies to match high frequencies Also FIR filter:
      D/A converter
- Can get better precision than RX
- Issues
  - How to set EQ weights?
  - Doesn't help loss at f
Transmit Linear Equalizer: Single Bit Operation

Example: 5Gbps Over 26” FR4 With No Equalization
Example: 5Gbps Over 26” FR4 Under Equalized

Example: 5Gbps Over 26” FR4 Over Equalized
Example: 5Gbps Over 26” FR4 Correct Tx Equalization

Decision Feedback Equalization

- Don’t invert channel... just remove ISI
  - Know ISI because already received symbols
  - Doesn’t amplify noise
  - Has error accumulation problem
    - Less of an issue in links where random noise small
- Requires a feed-forward equalizer for precursor ISI
  - Reshapes pulse to eliminate precursor
Alternate Approaches: Multi-Level Signaling

- Binary (NRZ) is 2-PAM
- 2-PAM uses 2-levels to send one bit per symbol
- Signaling rate = 2 x Nyquist
- 4-PAM uses 4-levels to send 2 bits per symbol
- Each level has 2 bit value
- Signaling rate = 4 x Nyquist

Note: both can be either single-ended or differential

When Does 4-PAM Make Sense?

- First order: slope of S21
  - 3 eyes: 1 eye = 10dB
  - loss > 10dB/octave: 4-PAM should be considered
Alternate Approaches: Simultaneous BiDirectional

- Two signals at half speed
  - Makes sense if b/w need equal in both directions

- Issues
  - Getting ideal timing between TX & RX is tough

Key Components In Links

- Background
- The Problem
- Key components
  - Loss: Equalization, MLS
  - Reflections: Termination, active methods
  - Skew: Clocking and PLLs, CDRs
  - TX & RX Design

- Results
- Future areas
Minimizing Reflections: The Vias

- Minimizing via stubs
  - Thinner PCBs are better… but sometimes impossible
  - Counter-boring
  - Blind vias
  - SMT technology

- All are costly
  - 1.1x - 2x

Vias: Effect of Counter-boring

- Counter-boring top layer takes it from highest-loss to lowest-loss & reduces resonance
Minimizing Reflections: Termination Design

- On-chip termination
  - Bondwire & pad capacitance part of the channel
  - Instead of a stub (which rings)

Minimizing Reflections: Terminating AC or DC

- With differential signals can terminate to the compliment
  - Potential power savings
    - Can build a higher-Z system
  - What sets common-mode?
    - Usually TX
    - Demands large RX common-mode range
  - AC-coupled & AC-term
    - Can set common mode with parallel large R’s

UC Berkeley EE241  J. Zerbe / B. Nikolic
Minimizing Reflections: FET Terminations

- (a) Diode
- (b) Two-Element
- (c) Fuzz-Gate
- (d) Digital Trimming

IV-characteristic of two-element resistor

Minimizing Reflections: Active Techniques

- Use sampled data stream to actively cancel reflections
Key Components In Links

- Background
- The Problem
- Key components
  - Loss: Equalization, MLS
  - Reflections: Termination, active methods
  - Skew: Clocking and PLLs, CDRs
  - TX & RX Design
- Results
- Future areas

Clocking: Terminology

- Synchronous
  Every participant gets same frequency and phase.

- Mesosynchronous
  Every participant gets same frequency, but unknown phase. Requires a way to recover the phase from the data. Coding (e.g., 8b/10b) is often used to make sure there are sufficient data edges.
  Can do with or without CDR

- Plesiosynchronous
  Every participant gets nearly the same frequency, slowly drifting phase. Requires a way to detect when the Rx clock has drifted 1/2 cycle from Tx clock.
  Needs CDR!

- Asynchronous
  Dispense with clocks altogether, use (e.g.) request/acknowledge 4-phase handshake to ensure correct sequencing of events.
What’s a CDR? Clock and Data Recovery

- Recovering clock from the data
  - Can recover clock completely, or just phase
  - Just phase: need a reference clock
- Why?
  - Allows separate xtals on different boards
  - Don’t have to match trace lengths, delays
  - Easier system design / clock distribution
- Why Not
  - Expensive: takes area, power
  - Requires coding or transition density or training sequence
    – 8b10b coding uses 10b to xfer 8b of info; 20% BW loss

CDR : PLL Technique

- Simple bang-bang PLL
  - Observe data with phase detector
  - Filter Early/Late & drive VCO
- Advantages
  - Good frequency range
  - Low Jitter
- Challenges
  - Phase offset
  - Lock time - startup sequence
  - Loss of lock - coding dependant
  - How to integrate?
    Multiple PLLs
    -Harmonic locking problems
**CDR : Dual-Loop Technique**

- Combination of
  - Core PLL provides multiple phases at frequency
  - Periphery DLL mixes and make desired phase

- Advantages
  - Avoids harmonic locking
    - Easy to integrate many
  - Rapid CDR lock time
  - CDR very stable
    - Can even 'hold' phase state

- Challenges
  - Limited Freq offset from PLL
  - Jitter not as low as PLL

**CDR : Coding & Transition Density**

- CDR requires transition density to keep lock
- AC - coupling requires DC-balance
- Coding as solution
- Typical code : 8b10b
  - 8 bits into the link => 10 bits on the wires
  - Raw data rate must be 25% faster than effective data rate
    - 6.25Gb raw for 5Gb effective
  - 8b10b code guarantees
    - DC balance
    - Transition density : 2 transitions every 10 bits
    - Reserved codes, control characters
  - CDR doesn’t mean you must have 8b10b
    - 64/66 or scrambling can give transition density
Key Components in Links

- Background
- The Problem
- Key components
  - Loss: Equalization, MLS
  - Reflections: Termination, active methods
  - Skew: Clocking and PLLs, CDRs
  - TX & RX Design
- Results
- Future areas

Transmitter Design

- Critical components: Sync, Mux, Tx
- Design issues:
  - Slew rate control vs ISI, jitter
  - Output current and impedance control
- Clock and Driver power dissipation
Output Drivers

(a) SSTL

(b) SSTL

(c) SSTL

(d) SSTL

I_o = +/- 8mA

I_o = +/- 16mA

V_{TT} = 0.45*V_{DDQ} (center term)

SSTL

Class-I

Class-II
**LVDS**

$I_o = \pm 3.5\text{mA}$

$V_{CM} = 1.25\text{V}$ (set by driver)

AC terminated @ receiver

---

**CML - direct coupled**

$I_o = -21\text{mA}$

Double-terminated on-chip
CML - AC coupled

\[ I_0 = -21mA \]

Supports different on-chip Vterms

Physical signal swings

\[ V_{DD} = 2.0V, 1.5V, 1.0V, 0.5V, 0V \]

CTT, SSTL, HSTL, TTL, GTL, GTL+, BTL, RSL, LVDS, CML

1 swing @ receiver input, driver swing will be higher.
2 differential signalling
Simple Transmitter

- DDR: send a bit per clock edge
- Critical issues:
  - 50% duty cycle
  - Tbit > 4-FO4

Fastest Transmitter

- Off chip time constant smaller than on chip:
  - Generate current pulse at the output
  - Limited only by the output capacitance

- Limiting time constant 25-Ω*Cpad
- Cpad = 8*Cdriver + Cesd
Simple Receiver

- Preconditioning stage: filter/integrate rectify CM
- Latch makes decision (4-FO4)
- DAC can be used to compensate offsets

Fastest Receiver

- Use multiple input receivers
  - Simplest 2, more complex 4-8
  - Decouples Tbit from latch resolution
  - Leverage high input impedance amplifiers
Measured Link Results

- Background
- The Problem
- Key components
- Results
- Future areas

Characterization System

- Multiple
  - Connectors
  - Backplane materials
  - Trace lengths
  - Layers/via lengths
  - Via technology
- These slides
  - 20” Trace length
  - FR4 non counter-bored
  - Nelco 6000 2-step counter-bored
  - Top & bottom layers

- 20” = 14” Backplane + 2 x 3” Linecards
- Linecards always FR4
Measured S21's: FR4 no C-Bore

![Graph showing measured S21's for FR4 no C-Bore](image)

26” FR4 Bot  3.125Gbps, 2P no EQ

![Graph showing 3.125Gbps data for FR4 Bot](image)
26” FR4 Bot  3.125Gbps, 2P  w/ EQ

26” FR4 Bot  6.4Gbps, 2P  w/ 3G EQ
26” FR4 Bot  6.4Gbps, 2P  w/ EQ

26” FR4 Top  6.4Gbps, 2P  w/ EQ
26" FR4 Top 6.4Gbps, 4P w/ EQ

Measured S21's: N 6k C-Bore
26” N6k-cb Top  6.4Gbps, 2P

10G Eyes & System Margin Shmoos

- 3”/20”/3” = 26” Trace + 2 Connectors
- Tested to BER < 10^{-15}
Future Areas for Work

- Background
- The Problem
- Key components
- Results
- Future areas
  - System Issues vs. Frequency
  - Link performance, power & area
  - Circuit challenges

System Issues vs. Frequency

<table>
<thead>
<tr>
<th>Voltage</th>
<th>100M</th>
<th>1G</th>
<th>3G</th>
<th>5G</th>
<th>10G</th>
</tr>
</thead>
<tbody>
<tr>
<td>Impedance matching across transmission line</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Return current path control</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reflection control</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Device I/O capacitance act as LPF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSN / Ground bounce</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cross talk</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Connector stub</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Skin effect</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dielectric loss</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inter symbol interference</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Via stub effect</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Timing</th>
<th>100M</th>
<th>1G</th>
<th>3G</th>
<th>5G</th>
<th>10G</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timing variation between clock and data</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timing variation across all pins</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timing variation due to coupling</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISI jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intra pair skew</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Link Performance vs. Time

- Serial Link Speed vs. Year of Publication (ISSCC)
- Internet Host Count vs. Year of Publication (ISSCC)
- Link Efficiency: Gb/W, Gb/mm²

Graphs showing trends and performance metrics for links over time.
## Next Challenges

- Improving PSR of all ckts in the path
- Integration of many links
  - Low power, area, portable solutions
- Control of complex architectures
  - Deal with loss, reflections and crosstalk
- Offset and mismatch
  - Both voltage and time

- Lots of opportunity for design!