EE241 - Spring 2003
Advanced Digital Integrated Circuits

Lecture 6
MOS Logic Styles

Reading

- Chapter 7 in the text by K. Bernstein
- Background material from Rabaey
- References
CMOS Logic Styles

- CMOS tradeoffs:
  - Speed
  - Power (energy)
  - Area

- Design tradeoffs
  - Robustness, scalability
  - Design time

- Many styles: don’t try to remember the names – remember the principles

---

Complementary

- Robust
- Scales large and slow

Pass Transistor Logic

- Simple and fast
- Not always very efficient
- Versatile
CMOS Logic Styles

Ratioed Logic

Dynamic Logic

small & fast static power

Static CMOS

Complementary CMOS

PMOS Only

NMOS Only
Complementary CMOS

- Very robust, full swing, high noise margins
  » But … high noise generation
- Fast to design, can synthesize
- Implements all logic functions
- No static power
- Among other properties:
  » Different pull-up and pull-down delays
  » Delay dependence on history
  » Crowbar current
  » Input capacitance consists of both P and N
  » Fast NAND, NOR, slow MUX, XOR

Complementary CMOS

UC Berkeley EE241

J. Rabaey, B. Nikolić


J. Rabaey, B. Nikolić
Transfer Function and Noise Margin

VTC of Complementary CMOS Gates
Body Effect

Delay Dependence on Input Patterns

<table>
<thead>
<tr>
<th>Input Data Pattern</th>
<th>Delay (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A=B=0→1</td>
<td>67</td>
</tr>
<tr>
<td>A=1, B=0→1</td>
<td>64</td>
</tr>
<tr>
<td>A=0→1, B=1</td>
<td>61</td>
</tr>
<tr>
<td>A=B=1→0</td>
<td>45</td>
</tr>
<tr>
<td>A=1, B=1→0</td>
<td>80</td>
</tr>
<tr>
<td>A=1→0, B=1</td>
<td>81</td>
</tr>
</tbody>
</table>

NMOS = 0.5μm/0.25 μm
PMOS = 0.75μm/0.25 μm
C_L = 100 fF
Propagation Delays

Pulsed Static CMOS

Bring circuit in known state before transition

Chen, Ditlow, US Pat. 5,495,188  Feb. 1996

Fast pull-up

Fast pull-down
**PS-CMOS**

- Advantages:
  - No dynamic nodes – good noise immunity
  - High static performance (monotonic)
  - No data dependent delay (worst case gets better)
  - No false transitions (monotonic)
  - Smaller clock load than dynamic

- Disadvantages
  - Width of reset wave limits logic depth and clock speed
  - Restricted connectivity
  - Complex clocking
Skewing Gates

- Different rising and falling delays

![Gate Diagrams]

Good for H-to-L transition  
Good for L-to-H transition

Ratioed Logic

(a) resistive load  
(b) depletion load NMOS  
(c) pseudo-NMOS

Goal: to reduce the number of devices over complementary CMOS
Pseudo-NMOS

Trade-off between performance and power + noise margins

Differential Logic
Differential Logic

- Differential Cascode Voltage Switch (DCVS)
- Differential Split-Level (DSL)
- Cascode Non-Threshold Logic (CNTL)
- Regenerative Push-Pull Cascode Logic (PPCL)
- Pass transistor logic families
- Dynamic logic families

Differential Logic

- Reduced logic depth + implicit invert, higher logic density

<table>
<thead>
<tr>
<th>Logic Function Capability (4 bit ALU)</th>
<th>CMOS (NAND)</th>
<th>ECL</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total circuit count</td>
<td>98</td>
<td>57</td>
<td>1.7</td>
</tr>
<tr>
<td>Circuit stages in signal paths(avg)</td>
<td>8.1</td>
<td>2.9</td>
<td>2.1</td>
</tr>
</tbody>
</table>

But
- Increased activity
- Routing
Cascode Voltage Switch Logic

Cascode Voltage Switch Logic (CVSL)

Sometimes called Differential Cascode Voltage Switch Logic (DCVSL)

CVSL

Fast (but hysteresis due to latch function)
No static power dissipation
BUT: large cross-over current!
CVSL

Full adder design

How to design for reduced transistor count?

Karnaugh Map Technique

Example: $Q = x_1x_2 + x_2x_3 + x_3x_1$

Connect "0" tree to $\overline{Q}$
"1" tree to $Q$
Karnaugh Map Technique

Example

\[ Q = x_1x_2x_3x_4 + x_1(x_2+x_3+x_4) \]
Using Ordered BDDs

Example: \[ f = x_1 x_2 + x_2 x_3 + x_3 x_1 \]
\[ = x_1 (x_2 + x_3) + x_3 (x_1 x_2) \]

Push-Pull Cascode Logic

**DSL Differential Split-Level Logic**

Idea:
Reduce logic swing at nodes q and q'

Assume:
- $V_{ref} = V_{dd}/2 + V_T$
- $V_{max} \text{ at q, q}' = V_{dd}/2$

**But ... Consumes Static Power**

- $T_3-T_4$ chain on
- $10 \text{ reduced logic}$
- $2 \text{ make } T_2 \text{ small}$

- performance: reduced swing $\rightarrow T_3 \rightarrow T_4$
- $T_3 \text{ in edge of conduction (almost off)}$
- $T_2 \text{ switch from high to high current mode}$
Simulation Results for Different Adders

<table>
<thead>
<tr>
<th>PROPERTY</th>
<th>STATIC FULL CMOS</th>
<th>STATIC DCVS</th>
<th>STATIC BSL</th>
<th>MODIFIED KIRK</th>
<th>DCVS REPAL</th>
<th>DCVS REPBD</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT Gate CAPACITANCE (pF)</td>
<td>155</td>
<td>85</td>
<td>85</td>
<td>110</td>
<td>85</td>
<td>85</td>
</tr>
<tr>
<td>OUTPUT LOAD CAPACITANCE (pF)</td>
<td>155</td>
<td>85</td>
<td>85</td>
<td>220</td>
<td>170</td>
<td>170</td>
</tr>
<tr>
<td># OF ACTIVE DEVICES</td>
<td>15/15</td>
<td>4/18</td>
<td>4/22</td>
<td>12/10</td>
<td>12/26</td>
<td>12/24</td>
</tr>
<tr>
<td>HIGHEST CASE RELAY TIME (ns)</td>
<td>20</td>
<td>22</td>
<td>14</td>
<td>18</td>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>AVERAGE POWER CONSUMPTION AT MAX. FREQ. (mW)</td>
<td>0.58</td>
<td>1.11</td>
<td>1.35</td>
<td>0.83</td>
<td>1.24</td>
<td>1.75</td>
</tr>
<tr>
<td>NORMALIZED POWER-DELAY PRODUCT</td>
<td>1.00</td>
<td>2.11</td>
<td>1.63</td>
<td>1.29</td>
<td>1.06</td>
<td>1.36</td>
</tr>
</tbody>
</table>

UC Berkeley EE241  J. Rabaey, B. Nikolić

Cascode Non-Threshold Logic

Use negative feedback to limit LOH
Capacitors used for decoupling
Optimizing the Intrinsic RC-Delay

1) Transistor Sizing
Make transistors wider
\( \rho \sim L/W \rightarrow R \downarrow \)

\[ C = 2C_D + C_g \]

but: \( C \uparrow \) - diffusion capacitance
- gate capacitance
sidewall capacitance remains unchanged
\( \rightarrow \) win, but not linear!

Progressive Sizing
Uniform versus Progressive Sizing

### Sizing Models

**Model 1: Uniform Scaling**

\[ t_p^U = 0.69 \cdot R \cdot C_L \cdot \frac{N}{k^{N-1}} + 0.69 \cdot R \cdot C \cdot \frac{N \cdot (N+1)}{2} \]

**Model 2: Non-uniform Scaling**

\[ t_p^N = 0.69 \cdot R \cdot C_L \cdot \left(1 + \frac{1}{k} + \frac{1}{k^2} + \ldots + \frac{1}{k^{N-1}}\right) + 0.69 \cdot R \cdot C \cdot \left(\frac{n \cdot (n-1)}{k} + \frac{n-1}{k^2} + \ldots + \frac{1}{k^{N-1}}\right) \]

\[ = 0.69 \cdot R \cdot C_L \cdot \left(1 - \frac{k^{-N}}{1 - k^{-1}}\right) + 0.69 \cdot R \cdot C \cdot \left(\frac{k^{-1} \cdot (1 - k^n - (k^n \cdot n) + k^{n+1} \cdot n)}{(k-1)^2}\right) \]
Case Study

Assume: $k = 1.2$

Table 1:

<table>
<thead>
<tr>
<th>N</th>
<th>Uniform</th>
<th>Non-uniform</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1.66</td>
<td>1.83</td>
</tr>
<tr>
<td>4</td>
<td>2.31 (1.7x)</td>
<td>3.1</td>
</tr>
<tr>
<td>6</td>
<td>2.41 (2.5x)</td>
<td>3.99</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td>2.83</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>8.46</td>
</tr>
<tr>
<td>6</td>
<td>21</td>
<td>16.05</td>
</tr>
</tbody>
</table>

Example: Progressive Scaling of NMOS Devices in DOMINO CMOS
What if External Capacitance is Dominant?

\[ t_p \sim R_{EQ} C_L \]

Divide and Conquer!

- Increasing \( I_{AV} \) \( \rightarrow \) larger W/L
- \( t_{sl} \)
- \( C_{IN} \) \( \rightarrow \) \( t_p \) (affects input slope)