Abstract

It is predicted that at the 90nm technology node, leakage power will exceed dynamic power. This poses several challenges to high-speed circuit designers. By the same token, the complexity of low power, low operating frequency designs is threatened more and more by static power dissipation concerns. It has been recently shown [1][2] that if energy per operation (EOP) is used as an optimization metric, then for a given microarchitecture, an optimal choice of $V_{dd}$ exists. However, throughput constraints are considered in this design only a-posteriori, and are not included in the optimization problem. In this project, we aim to extend these results, bringing architectural considerations into the game. The design and implementation of a digital filter, running at frequencies in the 1-10 MHz range, to be used as a decimator in a sigma-delta modulator, will be used a case study. Different architectural solutions (FIR, IIR, serial) will be compared from the point of view of the optimal-EOP $V_{dd}$ point, the goal being to design a filter architecture that can run at the optimal EOP point, while at the same time meeting the required throughput constraints. In addition, we will also investigate scalability of such attempt as we increase the operating frequency beyond the 1-10Mhz range. Designs obtained through this process will also be compared to the designs synthesized using a convex-optimization based tool.

PROJECT OUTLINE

Broadly speaking, the project will have the following steps:
1) Library characterization of the $V_{dd}$–$t_p$ curves of inverters, 2 and 3 input NAND gates (to consider the effect of stacking), EOP-optimal point in a multi-threshold technology, temperature and process corner dependency of the EOP-optimal point.
2) Architecture modeling: Estimating the complexity and clock frequency requirements of different architectures, pipelining/parallelization effect.
3) Architecture level EOP-optimal design.
4) Comparison with fully automated synthesis.
5) Physical design.

REFERENCES