EE241 - Spring 2006
Advanced Digital Integrated Circuits

Lecture 2: Scaling and Modeling

Device Models
### Basic CMOS Gate

**Properties**
- Output levels determined by supply
- Large noise margins
- Performance loss at low voltages (overdrives)

![CMOS Gate Diagram](image)

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### Digital Gate

**Basic Properties**

- Functionality
- Area (Cost)
  - Density
- Robustness
  - $\Delta$ Swing, Noise margins, Noise sensitivity
- Delay
  - $t_{PLH}$, $t_{PHL}$
- Power, energy consumption
Transistor Models

- In this class we will use a variety of transistor models
- Always use the simplest one needed to analyze a particular effect

The MOS Transistor

MOS transistor with biasing
Transistor Modeling

- Different levels:
  - Hand analysis
  - Computer-aided analysis (e.g. Matlab)
  - Switch-level simulation (e.g. TimeMill)
  - Circuit simulation (Hspice)
- These levels have different requirements in complexity, accuracy and speed of computation
- We are primarily interested in delay and energy modeling, rather than current modeling
- But we have to start from the currents

MOS Current

- Vertical field set by $V_{gs}$ induces channel charge
- Gradual charge in the channel is assumed
- Fixed charge in the channel is completely cancelled at $V_{gs} = V_{th}$
- Charge in the channel is
  $$Q_n = C_{ox} (V_{gs} - V_{th} - V_{c}(x))$$
- By Ohm’s law,
  $$I_{ds} = WQ_n(x)v = WC_{ox} (V_{gs} - V_{th} - V_{c}(x)) \mu E$$
- Also $E = dV_c(x)/dx$
- Key assumption is that $v = \mu E$, and mobility ($\mu$) is constant
MOS Current

\[ I_{DS} = W C_{ox} (V_{GS} - V_{Th} - V_c(x)) \mu E \]
\[ I_{DS} = W C_{ox} (V_{GS} - V_{Th} - V_c(x)) \mu (V_c(x)/dx) \]

*When integrated over the channel:

\[ I_{DS} = \frac{W}{L} \mu C_{ox} \left( V_{GS} - V_{Th} - \frac{V_{DS}}{2} \right) V_{DS} \]

- Transistor saturates when \( V_{GD} = V_{Th} \), the channel pinches off at drain’s side.

\[ I_{DS} = \frac{W}{2L} \mu C_{ox} (V_{GS} - V_{Th})^2 \]
MOS Currents

Currents according to the quadratic model
Correct for long channel devices (L ~ μm)

Simulated 0.13μm Transistor

L = 0.13μm
Simulation vs. Model

Major discrepancies:
- shape
- saturation points
- output resistances

Velocity Saturation

- $v_{sat} = 10^5$
- $E_c = 1.5$
- Constant velocity
- Constant mobility (slope = $\mu$)
**Unified MOS Equations**

\[
I_D = \begin{cases} 
0, & V_{GS} < V_{TH} \\
\frac{k'}{L} \left( V_{GS} - V_{TH} \right) \frac{V_D^2}{2} & V_{GS} > V_{TH}, V_{DS} > V_{GS} - V_{TH}, V_{DSAT} > V_{GS} - V_{TH} \\
\frac{k'}{2L} (V_{GS} - V_{TH})^2 & V_{GS} > V_{TH}, V_{DS} > V_{GS} - V_{TH}, V_{DSAT} < V_{GS} - V_{TH} \\
\frac{k'}{L} \left( V_{GS} - V_{TH} \right) \frac{V_{DSAT}^2}{2} & V_{GS} > V_{TH}, V_{DS} > V_{GS} - V_{TH}, V_{DSAT} > V_{GS} - V_{TH} 
\end{cases}
\]

From EECS141
Rabaey, 2nd ed.

**MOS Models**

\[ I_D = \begin{cases} 
0 & V_{GT} \leq 0 \\
\frac{k'}{L} \left( V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) (1 + \frac{\lambda V_{DS}}{2}) & V_{GT} \geq 0 
\end{cases} \]

with \( V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT}) \),
\[ V_{GT} = V_{GS} - V_T, \]
and \[ V_T = V_{TH} + \gamma \sqrt{1 - 2\Phi_F + V_{SB}} - \sqrt{1 + 2\Phi_F} \]

\( \gamma \) - body effect parameter

From EECS141
Rabaey, 2nd ed.
Unified MOS Model

- Model presented is compact and suitable for hand analysis.
- Still have to keep in mind the main approximation: that $V_{DSat}$ is constant. When is it going to cause largest errors?
  - When $E$ scales – transistor stacks.
- But the model still works fairly well.

Velocity Saturation

- Velocity is not always proportional to field
- Modeled through variable mobility (mobility degrades at high fields)

$$v = \frac{\mu_{eff} E}{1 + \left(\frac{E}{E_0}\right)^{1/n}}$$

$$E_0 = \frac{2v_{sat}}{\mu_{eff}}$$

NMOS: $n = 2$
PMOS: $n = 1$

- Hard to solve for $n = 2$
- Assume $n = 1$ (close enough)

[Sodini84]
Velocity Saturation

When does a transistor enter velocity saturation?

\[ V_{DSat} = \frac{(V_{GS} - V_{Th})E_{CL}}{(V_{GS} - V_{Th}) + E_{CL}} \]  

[Taur, Ning]

- \( E_{CL} \) is a function of vertical field, \(~\text{linearly proportional to}~ V_{GS} \)

In 0.13\( \mu \)m technology, \( E_{CL} \) is about \( 0.5V_{GS} + 0.7V \)

Can calculate \( V_{DSat} \) \( \left( V_{Th} \sim 0.25V \right) \)

<table>
<thead>
<tr>
<th>( V_{gs} [V] )</th>
<th>0.2</th>
<th>0.4</th>
<th>0.6</th>
<th>0.8</th>
<th>1.0</th>
<th>1.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DSat} [V] )</td>
<td>0</td>
<td>0.13</td>
<td>0.26</td>
<td>0.37</td>
<td>0.46</td>
<td>0.55</td>
</tr>
</tbody>
</table>

- For \( V_{GS} - V_{Th} \ll E_{CL} \), \( V_{GS} < 1V \)
  \( V_{DSat} \) is close to \( V_{GS} - V_{Th} \)
- For large \( V_{GS} \), \( V_{DSat} \) would start bending upwards toward \( E_{CL} \), but we won’t even notice it with 1.2V supply.
- Therefore \( E_{CL} \) can be frequently approximated with a constant term \( (E_{CL} = 1.2V \text{ in } 0.13\mu m) \)
**Velocity Saturation**

![Graph showing velocity saturation](image)

**Drain Current**

We can also find the current

\[ I_{DSat} = v_{Sat} W C_{ox} \left( \frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_C L} \right) \]

- Good model, could be used in hand or Matlab analysis

\[ I_{DSat} = \frac{W \mu_{eff} C_{ox} E_C L}{2} \left( \frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_C L} \right) \]

\[ I_{DSat} = \frac{W \mu_{eff} C_{ox}}{2} V_{DSat} (V_{GS} - V_{Th}) \]
Drain Current

Output Resistance

- Slope in I-V characteristics caused by:
  - Channel length modulation
  - Drain-induced barrier lowering (DIBL)
- Both effects increase the saturation current beyond the saturation point
- The simulations show approximately linear dependence of $I_{ds}$ on $V_{ds}$ in saturation.

[BSIM 3v3 Manual]
Output Resistance

- **Channel length modulation**
  - As the drain voltage increases beyond the saturation voltage $V_{dsat}$, the saturation point moves slightly closer to the source ($\Delta L$)
  - The equation is modified by replacing $L$ with $\Delta L$
  - Taylor expansion $I_{ds} = I_{dsat}(1 + V_{ds}/V_A)$

![Diagram of MOSFET showing channel length modulation](image)

Output Resistance

- **DIBL**
  - In a short channel device, source-drain distance is comparable to the depletion region widths, and the drain voltage can modulate the threshold
  - $V_{Th} = V_{Th} - \xi V_{ds}$
  - Taylor expansion

![Graph showing output resistance for long and short channels](image)
NAND Gate

- 2-input NAND gate

Sizing for equal transitions:
- P/N ratio (β-ratio) of 2 (more about this later in the class)
- Upsizing stacks by a factor proportional to the stack height

Transistor Stacks

- With transistor stacks, $V_{DS}$, $V_{GS}$ reduce.
- Unified model assumes $V_{DSat} = \text{const.}$
- For a stack of two, appears that both have exactly double $R_{ekv}$ of an inverter with the same width
- Therefore, doubling the size of each, should make the pull down $R$ equivalent to an inverter
Velocity Saturation

As \((V_{GS} - V_{Th})/E_CL\) changes, the depth of saturation changes

\[
I_{DSat} = \frac{W \mu_{eff} C_{ox} E_CL}{L} \frac{(V_{GS} - V_{Th})^2}{2} \frac{(V_{GS} - V_{Th}) + E_CL}{E_CL}
\]

- For \(V_{GS}, V_{DS} = 1.2V, E_CL\) is 1.3V
- With double length, \(E_CL\) is 2.6V (in this model)
- Stacked transistors are less saturated
- \(V_{GS} - V_{Th} = 0.95V, I_{DSat} \sim 2/3\) of inverter \(I_{DSat}\) (63%)
- Therefore NAND2 should have pull down sized 1.5X
- Check any library NAND2’s

How about NAND3?

\(I_{DSat} = 1/2\) of inverter \(I_{DSat}\) (instead of 1/3)

How about PMOS networks?

- NOR2 – 1.8x, NOR3 – 2.4x, NOR4 - 3.2x
- What is \(E_CL\) for PMOS?
**Alpha Power Law Model**

- Alternate approach, sometimes useful for hand analysis

\[ I_{DS} = \frac{W}{2L} \mu C_{ox} (V_{GS} - V_{Th})^\alpha \]

- Parameter \( \alpha \) is between 1 and 2.
- In 0.13 - 0.25µm technology \( \alpha \sim 1.2 \).

[Sakurai, Newton, JSSC 4/90]

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**Alpha Power Law Model**

- This is not a physical model
- Simply empirical:
  - Can fit (in minimum mean squares sense) to variety of \( \alpha \)'s, \( V_{Th} \)
  - Need to find one with minimum square error – fitted \( V_{Th} \) can be different from physical
  - Can also fit to \( \alpha = 1 \)
    - What is \( V_{Th} \)?
$K(V_{GS} - V_{THZ})$ Model

Drain current vs. gate-source voltage

Transistor Leakage

Leakage current is exponential with $V_{GS}$

$V_{DS} = 1.2V$
Transistor Leakage

Two effects:
- diffusion current (like a bipolar transistor)
- exponential increase with $V_{DS}$ (DIBL)

slope factor $S = kT/q \ln 10(1 + C_d/C_i)$

$kT/q$ 60mV/decade

$C_d$ depletion layer cap

$C_i$ gate oxide capacitance

Typical value $S \sim 70$-90mV

$V_T >> S$

Solution: Newer device structures

Eg: thin film SOI transistors with fully depleted channels
Subthreshold Current

- Subthreshold behavior can be modeled physically

\[
I_{ds} = \mu \frac{W}{L} \left( \frac{kT}{q} \right)^2 e^{\frac{V_g - V_{Th}}{m k T / q}} \left( 1 - e^{-\frac{V_{ds}}{kT/q}} \right)
\]

Or:

\[
I_{ds} = I_0 \frac{W}{W_0} 10^{\frac{(V_{gs} - V_{Th}) + \gamma V_{ds}}{s}}
\]

[Taur, Ning]

Leakage Components

![ Leakage Components Diagram ]

Leakage Components

1. 
   2. 
   3. 
   4. 
   5. 
   6. 
   7. 
   8. 

porate

Drain-induced barrier lowering (DIBL)
Gate-induced drain leakage (GIDL)

leakage

Gate oxide tunneling
Hot carrier injection
DIBL, GIDL, Weak Inversion

![Graph showing DIBL, GIDL, and Weak Inversion effects in MOSFETs.](image)


Stack Effect

NAND gate:

![NAND gate circuit diagram](image)

Reduction:

<table>
<thead>
<tr>
<th></th>
<th>High $V_i$</th>
<th>Low $V_i$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 NMOS</td>
<td>10.7X</td>
<td>9.96X</td>
</tr>
<tr>
<td>3 NMOS</td>
<td>21.1X</td>
<td>18.8X</td>
</tr>
<tr>
<td>4 NMOS</td>
<td>31.5X</td>
<td>26.7X</td>
</tr>
<tr>
<td>2 PMOS</td>
<td>8.6X</td>
<td>7.9X</td>
</tr>
<tr>
<td>3 PMOS</td>
<td>16.1X</td>
<td>13.7X</td>
</tr>
<tr>
<td>4 PMOS</td>
<td>23.1X</td>
<td>18.7X</td>
</tr>
</tbody>
</table>