The limited switch dynamic logic (LSDL) logic family merges dynamic logic and static latches with the intent of reaping the speed advantages of dynamic logic while avoiding the dynamic power penalty. Standard domino logic requires precharging of the dynamic output node every cycle, meaning that the output will often have to switch every cycle even though its logic value remains constant. LSDL inserts a static latch and between the dynamic node and the load, greatly reducing the capacitance load of the dynamic node. This in turn reduces the required size of the pre-charge PFET, reducing the capacitance load of the clock.

The hope in using LSDL is that the power-performance-area tradeoff may be shifted favorably. However, no systematic studies have been published benchmarking LSDL against other logic families.

In this project, I propose to implement a simple circuit (any suggestions? perhaps an 8-bit carry look-ahead adder?) in static, domino, and LSDL logic, and compare the power-performance-area tradeoffs in the three logic styles.