Self-tuned, Self-timed State Machine Design Using Low Power Pass Transistor Technology

With scaling leading to shorter and shorter channel lengths, leakage power is becoming a dominant factor in designing reliable circuits. Typical static CMOS design leaves a small number of devices between the power and ground rails resulting in a large quiescent leakage current. In some cases the leakage power is similar to the peak dynamic power. Pass transistor technology shows promise in drastically reducing these leakage currents by not allowing paths from power to ground through a small number of transistors.

Pass transistor logic generally is not used because it can lead to long delay paths. However, since the leakage currents are reduced the threshold voltage can be reduced to regain some of the performance loss. A library based around this pass transistor logic is under development at the BWRC. Currently it is used for regular logic structures and datapath elements. I will examine the possibility of extending its use to more random control logic, specifically state machines. I hope to extend the idea even further into making the state machine self-timed and self-tuned.