Design Considerations for Logic Operating in the IC = 1 Regime

Cristian Marcu, Michael Mark, Jesse Richmond
UC Berkeley
Proposal for the EE241 Spring 2006 Class Project

For a long time performance has been the main innovation driver for digital circuits. However, due to the constant increase in speed and complexity and the demand for mobile devices, energy issues like power consumption and self-heating of the chips have turned out to be major limiting factors in the everlasting quest for higher speeds. Due to these limiting factors, we have started to observe a saturation of microprocessor speeds and a move toward concurrent computing as a way to increase overall system performance.

At the circuit level a lot of research has been done recently on logic design in weak inversion (IC<<1), which has been proven to be extremely power efficient with respect to conventional logic operating in strong inversion (IC>>1) [Vittoz]. Unfortunately, weak inversion is at an inherent disadvantage in speed, which may prevent its use in applications requiring high-speed logic.

In analog design, MOS transistors operating in moderate inversion (IC=1) which trade-off between speed (strong inversion) and power (weak inversion), are already widely used for low-power circuits up to frequencies of several GHz. We are planning to establish a similar trade-off between the regions of inversion in the digital domain. During the course of this project we are planning to do some theoretical investigation on logic operating in the IC = 1 regime in order to come up with some appropriate design guidelines. A main part of this work will be to provide some decision thresholds for the optimal region of operation for given power and speed constraints. The other main component of this work will be to actually implement our ideas in some circuit designs. We are planning to implement our design strategy using the case of a standard building block (e.g. adder or multiplier) and compare it to the same building block operating in weak and in strong inversion in order to confirm our theoretical considerations, including any special design challenges we encounter with moderate inversion transistors.