1. **CTLE design and performance:** In this problem we will look at a CTLE within a link operating over a channel that can be modeled as a simple first-order low-pass filter with a pole $\omega_p = 2\pi*1$GHz and a fixed transmit swing of 200mV differential peak-to-peak. You can also assume that the input devices in the CTLE have infinite $r_o$, $V^*$ of 200mV, $\omega_T = 2\pi*60$GHz, and $\gamma_{drn} = \frac{C_{dd}}{C_{gg}} = 0.8$.

   a. If the CTLE must drive a fixed load capacitance of $C_L = 25fF$ and must always maintain an output swing of 50mV differential peak-to-peak, plot the peak gain (i.e., $g_m^*R_L$) and bias current of the CTLE vs. link data-rate ranging from 2Gb/s to 20Gb/s. Don’t forget to include the self-loading of the CTLE.

   b. Assuming that the noise of the CTLE is dominated by the input devices and that $\gamma_{noise} = 1$ for the devices, under the same conditions as part a., plot the $\sigma$ of the voltage noise at the output of the CTLE.

2. **FIR/DFE design:** In this problem we will examine the design of a DFE that will be used in a 10Gb/s link implemented in a 45nm technology which could potentially be operating over any one of the four channels shown below. Note that all of the taps values provided below are normalized to the swing of the transmitter. Throughout this problem, you can assume that all transistors in saturation have a $V^*$ of 200mV, $\omega_T = 2\pi*50$GHz, current density $I_{DSAT} = 38\mu A/\mu m$, and $\gamma_{drn} = \frac{C_{dd}}{C_{gg}} = 1$.

   a. Assuming that the transmitter has a swing of $+/-50$mV (i.e., 100mV differential peak-to-peak) and that your DFE must provide at least $+/-40$mV of swing due to the cursor (i.e., the voltage swing due to the remaining ISI taps is not included) at its output while driving a fixed capacitance of 20fF, design and sketch a DFE summer that would cancel the ISI of the first post-cursor over any of the 4 channels shown above. You can assume that the delay of the digital portion of the feedback is 40ps and that the DFE should settle to within $\sim$2% of its final value (i.e., $4\tau$ of analog settling), and you should provide device sizes as well as resistor values. You don’t need to
implement the current sources, but you should provide the value of the input stage current source, as well as the range of the values for the tap current source.

b. For your design from part a., what is the worst-case voltage margin over each of the four channels? In the worst case, how much power does the DFE summer consume?

c. Using the same design procedure you developed to solve parts a. and b., plot the worst-case voltage margin over each of the four channels as well as the worst-case power consumed by the DFE summer as you increase the number of taps in the feedback filter from 1 to 10. For this part of the problem you should assume that every non-zero tap you add must have its own current-steering pair – i.e., the only digital logic in the DFE should be a shift register.

d. In practice, every time you add another tap to the DFE summer, you also add some capacitance to the summer output node due to the extended length of the output wire. Repeat part c. but now assuming that every tap you adds 0.5fF of wire capacitance to the DFE summer’s output (in addition to the loading from the tap switches themselves).

e. **BONUS:** Noticing that many of the channels are “sparse” – i.e., have several post-cursor ISI taps whose value is zero, can you redesign the digital logic/DFE summer and reduce the overall power consumed by the DFE? In answering this question you should assume that the nominal $V_{dd}$ in this technology is 1V, that the FO4 delay of an inverter is 20ps, and that $R_{snp} = 2R_{sqn}$. Furthermore, you should assume that each flip-flop will place 10fF of equivalent loading on the 10GHz clock, and you should also be sure to include the power consumed by any combinational logic gates you add; if needed, you can assume that the minimum transistor width is 0.12µm.