Overview
The goal of this project is to design and evaluate a high-speed serial transceiver built in a 45nm CMOS technology operating in a backplane environment. Although a complete high-serial transceiver contains a broad variety of components and sub-systems, to the extent possible, this design will be carried out at the circuit/transistor-level. Further detail on the 45nm technology as well as setting up Cadence to utilize this technology will be posted on the web.

At a minimum, by the end of the project you should be able to demonstrate a functional behavioral model of the transceiver, but the more blocks/components you have complete implementations of, the better. Further guidance on block priorities and strategies for successful integration will be provided in this and future project handouts.

A sketch of the backplane environment your transceiver will be operating in is shown above. Each channel within the backplane can have widely varying characteristics, and hence a representative subset of 5 of these channels have been selected and provided to you (details in the next section) to use in evaluating the performance/functionality of your transceiver. Each channel traverses through the chip-package-PCB interface, two 3-inch line card traces, and with varying length and layer (top, middle, or bottom) on the backplane itself. The system is plesiochronous – i.e., there is a separate clock crystal on each line card.

We have intentionally provided you with very few specifications because understanding the tradeoffs inherent in the design of the transceiver circuits is an integral part of the project. The only specifications which all project teams must meet are as follows:
• Minimum data-rate (all channels): 10Gb/s
• Maximum BER (all channels): $10^{-15}$
• Maximum crystal reference frequency: 500MHz
• Maximum crystal frequency offset: +/- 20ppm
• Use of at most 2 independent external power supplies per transceiver (TX/RX pair)
• Meet BER spec under +/-25mV of peak-to-peak noise on each power supply (the spectrum of this supply noise will be provided at a later date)
• Operating temperature: 25° C

As long as your design meets the above requirements, you are free to explore the tradeoffs between data-rate and power consumption. However, no matter what data-rate you choose, you should be sure to minimize the power used to achieve this data-rate.

Phase 1 Tasks

For this first phase of the project, your first principal task will be to characterize the channels at various data-rates. Based on this characterization, you will then propose a preliminary set of targets for your design (e.g., highest bit-rate, lowest possible power, etc.). Finally, you will propose an initial equalization architecture as well as a plan for how you will characterize/validate the BER of the transceiver operating over the various channels.

i. Channel Characterization

The 5 channels you will be evaluating are posted on the class website in the zipped folder `channel_sim_files.zip`; you can also copy these files from the EE290C home directory on the instructional machines from:

/home/ff/ee290c/spring11/project/channel_sim_files

The main file you will use/modify to simulate and characterize the channels is `chan_template.sp`; as described in the comments in the file itself, you will need to add appropriate models for the transmitter and receiver (including their terminations). Note that once you have actually built the circuitry the channel may change slightly due to additional parasitics from the circuitry, so you may want to include a preliminary estimate of the TX/RX loading.

For this phase of the project you can assume that your transmitter and receiver circuits will provide ideal termination values (at least at DC). However, you should keep in mind that in practice you will only be able to set the termination values (especially if you use a voltage mode transmitter) to within finite accuracy. Thus, even for this preliminary stage of the project, you may want to consider the effects of +/-2% variation in the transmitter or receiver termination resistance.

Once you have set up the characterization deck, you should provide the following plots for each channel:

• AC magnitude and phase (i.e., s21) from 0Hz to 20GHz.
• Time-domain pulse response at 10Gb/s sampled with 2ps timing resolution and indicating symbol-spaced sample values.
• Time-domain pulse response at your target data-rate sampled with 2ps timing resolution and indicating symbol-spaced sample values.
ii. Design Targets Proposal

In this section you should provide a brief proposal of preliminary targets for your transceiver design. At a minimum, this proposal should include the target data-rate and power consumption for your design. However, since Elad will provide each team feedback on its proposal, the more detail you can provide in terms of how you plan to achieve these targets, the better. Examples of things you may want to include here are the type of transmitter you plan to use (voltage-mode vs. current-mode), transmit swing/common-mode, clocking strategy on both the TX and RX (full-rate, half-rate, etc.), equalization strategy/partitioning (see next section), clock recovery strategy, and power estimates.

iii. Equalization Architecture Proposal

In this section you should provide an initial proposal for the equalization strategy you plan to apply in order to ensure reliable operation at your target data-rate. For example, will you be using TX FIR, RX CTLE, DFE, some combination thereof, etc.? If you are using FIR or DFE, how many taps will each one include, and how will you adapt them? (Note that you can assume that you have a means to communicate information from the receiver back to the transmitter.)

Although not required for this phase of the project, it is highly recommended that you evaluate the efficacy (i.e., achievable voltage margin) of your proposed equalization architecture on all 5 of the channels and include plots of the equalized pulse responses (with coefficients set in an ideal manner) in your report.

iv. BER Evaluation Proposal

In this final section you should briefly describe the approach you plan to take in order to evaluate and validate the BER of your transceiver when it operates on each of the 5 channels. In particular, you should address whether you plan to apply worst-case analysis vs. full statistical calculations (note that full statistical analysis may or may not be necessary depending on the error characteristics), and you should briefly describe how you will extract from your final completed implementations the parameters you need to apply your methodology. You should also include a list of the error sources you plan to include when estimating BER.

Report Submission

All project phase 1 reports should be submitted by email to Elad; no hard copy reports will be accepted.