Overview
The principal goal of this phase of the project is to continue working on the circuit design of the transceiver, and in particular to ensure that you’ve started the design of the clock generation and recovery circuitry. While you will once again still have the opportunity to modify the circuits you design now later in the project, you should plan to have as many transistor-level designs of the critical components as possible completed by the end of this phase.

One important thing to note is that CDRs often contain a reasonable amount of digital logic, but that this logic is typically operated at relatively low speeds. In order to reduce scope, for this project you should feel free to write in behavioral verilog/VHDL (or any other hardware description language, HDL) any such digital logic you may need. In other words, you need not design at the transistor-level any of the digital control blocks (e.g., accumulators for the CDR/equalizer adaptation, edge or up-down detection logic, etc.) – in fact, you should feel free to write the serializers/deserializers in an HDL as well. You should however assume a “reasonable” loading/drive strength from these blocks. You also shouldn’t abuse this simplification and assume that complex, high-speed digital logic is free – keep in mind that at 10GHz it only takes ~10 flip-flops to dissipate 1mW.

You can assume that you are provided with a reference clock source with a frequency of up to 500MHz (i.e., you can use a lower frequency if you’d like, but your reference frequency can not be higher than 500MHz). You should also keep in mind that the frequency offset between the transmitter and the receiver can be up to +/-20ppm. In terms of the jitter/phase noise characteristics of this reference clock, you should perform a quick search on the web and use the characteristics quoted from commercial reference clock parts that you can buy. (Even if these parts can provide references at over 500MHz, you should use the phase noise quoted at 500MHz.) If you are unsure about where to look for these parts please contact Elad and he can give you some pointers.

Phase 3 Tasks
As previously mentioned, your principal task for this phase of the project is to complete preliminary transistor-level designs of the clock generation and recovery circuitry, and of course to continue working towards completing the signaling circuitry if you haven’t done so already. The first step will therefore be for you to write behavioral models of the critical components of the clock generation and recovery components. You should then combine these models along with your models (and/or complete designs) of the signaling path components to show that your sampling clock does indeed converge to an appropriate phase (and frequency) position. Finally, you should describe the methodology you will use to evaluate the impact on BER of your clock generation/recovery implementation.

i. Component Models
These models should once again capture the most relevant behavior of each block (but not necessarily second-order effects), and should be pin-compatible with the actual final implementation.

**ii. Transistor-Level Schematics**

The main goal of this task is to complete transistor-level schematics for the clock generation and recovery components. Although you should already have a pretty good idea what these circuits will be driving (since you should have nearly completed the signaling circuitry), you should keep in mind that you want/need to make modifications to these designs in the final phase of the project.

**iii. Clock Recovery/Generation Simulations**

Once you’ve completed the design and/or models of all of the clocking components, you should put them together along with the signaling path and simulate show that everything locks under the following scenarios:

1. 0ppm frequency offset, ½ UI initial timing error
2. TX 20ppm faster than RX, random initial timing error
3. RX 20ppm slower than TX, random initial timing error

Note that because of the widely varying time-scales involved you will most likely want to carry out these simulations using your behavioral models (or with co-simulation), and results based on these models will receive full credit. You should provide time-domain traces showing the locking behavior of your loops for each of the three scenarios above.

Note that your clock recovery simulation in particular should ideally be carried out with the actual channel model as well as all of your equalization/signaling circuitry. However, if you are unable to complete this full simulation during this phase of the project, you will still receive full credit (for this phase) by demonstrating the functionality of your loops on idealized input waveforms (with no ISI, noise, etc.).

**iv. BER Evaluation**

In this final section you should briefly describe the approach you plan to take in order to evaluate the impact of your timing circuitry on overall BER of your transceiver. In particular, you should address how you will estimate the effective jitter/timing errors, and whether you plan to apply separate timing vs. voltage budgets or include their interactions (e.g. as we discussed in lecture). You should also be sure to highlight how you will extract from your implementation any parameters you need to apply your methodology.

**Report Submission**

All project phase 3 reports should be submitted by email to Elad; no hard copy reports will be accepted.