Overview

The goal of this final phase of the project is simple – complete as much of the circuit and block design/verification of your link as possible. The only components you may not yet have included in your models are the adaptation loops to control e.g. the equalizer coefficients, and hence you should first add these in (as behavioral models and/or verilog). This should enable you to complete (behavioral) simulations with all of your loops – PLL, CDR, equalization, etc. – running together, and your report should include traces showing that these loops indeed lock. Once this is complete you should then focus on the (transistor-level) circuit design of all of the critical components, feeding the more detailed/accurate information you gain from these implementations into your overall link BER/power evaluation.

As with the earlier phases of the project, you should feel free to write behavioral verilog/VHDL models for any of the digital logic used in the control paths.

As a final reminder, you should be careful to include all sources of noise – including thermal, flicker, power supply, and dither from the various loops – in your performance/BER estimates. For supply noise, you should assume that each independent supply has +/-25mV of noise on it (relative to its ground), where the spectrum of that noise has been filtered by the second-order transfer function provided below:

\[ H(s) = \frac{1+s/\omega_n}{s^2/\omega_n^2 + (2\zeta/\omega_n)s + 1} \]

\[ \omega_n = 1Grps, \quad \omega_n = 1.91Grps, \quad \zeta = 0.348 \]

Note that for simulation or analysis purposes, you can generate this noise by passing a white voltage noise source through the above filter and then setting the spectral density of that white noise source (based on e.g. the simulation time-step you are using) so that the +/-4\sigma value of the noise after the filter is +/-25mV. Even though you will be using a random source to simulate the noise, for the purpose of analysis you can continue to assume that the noise is bounded at +/-25mV. Keep in mind that each supply voltage should have a separate such source – i.e., the noise on each of the power supplies is uncorrelated.

Phase 4 Tasks

i. Complete Link Model

By the completion of the project you should have all critical components of the link – signaling path, clocking, equalization, etc. – modeled behaviorally (if not implemented at the circuit level). You should then run the entire link and show the various coefficients/settings converging under each of the 5 channels.
ii. Transistor-Level Schematics

As previously mentioned, the main goal of this phase of the project is for you to complete as many transistor-level schematics of the actual link as possible. The more complete your circuits are – and hence the more accurate your estimates of the actual performance of your link – the better.

iii. Presentation

Before turning in the final report your group will give a presentation on the final complete design of the link. This presentation should focus on the overall architecture, the methodology you used to select this architecture (especially if it has expanded/changed since phase 2), and results from the circuits and complete system simulations (and how you arrived at these results). These presentations are mainly intended to serve as an opportunity to receive feedback/suggestions before submitting the final report; further details will be provided in lecture.

iv. Performance, Power, and BER Evaluation

Finally, your report should include a summary of the performance (data-rate and any other parameters of the sub-blocks that may be of interest) of the link, a power breakdown of the various components, and the predicted BER on each of the five channels. You should also be sure that the methodology you are using to predict BER has been clearly explained (either in this final and/or earlier reports).

Report Submission

All project phase 4 reports should be submitted by email to Elad; no hard copy reports will be accepted.