Embedded System Design for Wireless Applications

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DAC 2000, Los Angeles

The Distributed Approach to Information Processing

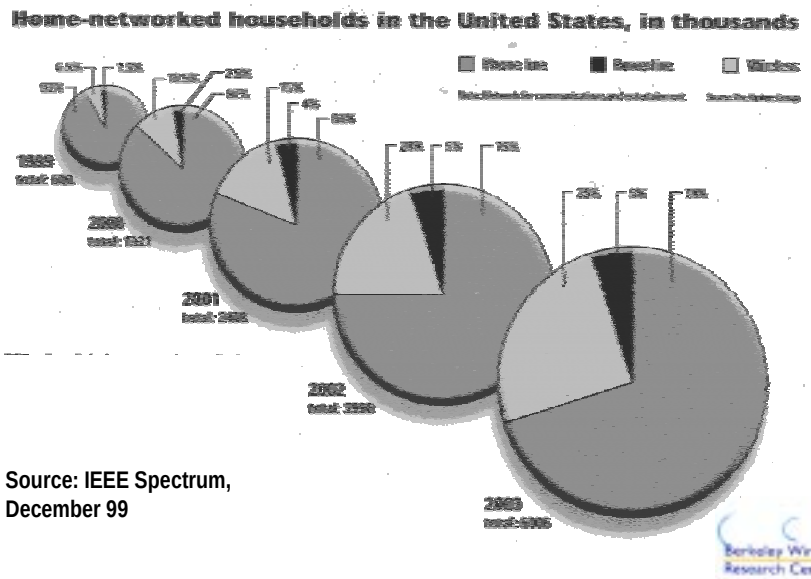
Source: Richard Newton

The Smart Home

Dense network of sensor and monitor nodes

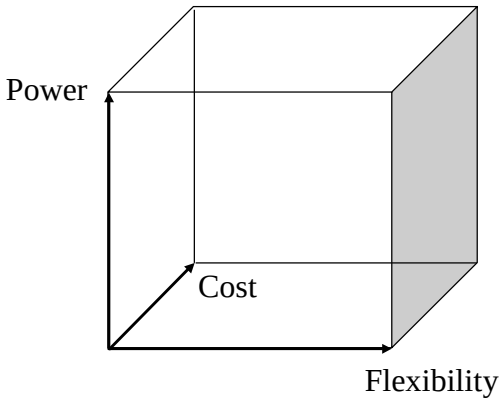
Security
Environment monitoring and control
Object tagging
Identification

Wireless in the Home



Source: IEEE Spectrum, December 99

The Changing Metrics



Performance as a Functionality Constraint
("Just-in-Time Computing")

The Wireless System Design Challenge

The Battery Limitation

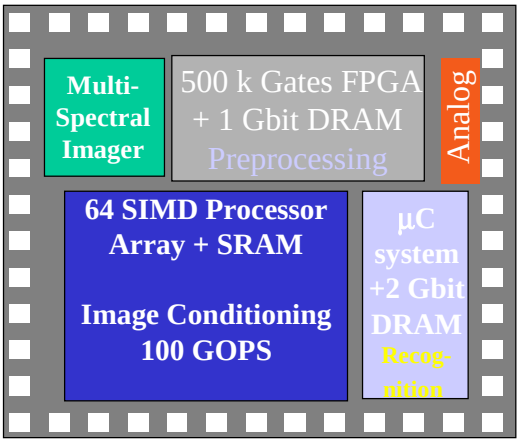
- **Projected energy per digital operation (2004): 50 pJ**
- **Lithium-Ion: 220 Watt-hours/kg == 800 Joules/gr**
- **At 50 pJ/operation:10 teraOps/gr!**
  - Equivalent to continuous operation at 100 MOPS for 30 hours (or average power dissipation of 6 mW)

Some interesting numbers

- **Energy cost of digital computation**
  - 1999 (0.25µm): 1pJ/op (custom) … 1nJ/op (µproc)
  - 2004 (0.1µm): 0.1pJ/op (custom) … 100pJ/op (µproc)
    - Factor 1.6 per year; Factor 10 over 5 years
    - Assuming reconfigurable implementation: 1 pJ/op
- **Energy cost of communication**
  - 1999 Bluetooth (2.4 GHz band, 10m distance)
    - 1 nJ/bit transmission energy (thermal limit 30 pJ/bit)
    - Overall energy: 170 nJ/bit reception / 150 nJ/bit transmission (!)
    - Standby power: 300 µW
  - 2004 Radio (10 m)
    - Only minor reduction in transmission energy
    - Reduce transceiver energy with at least a factor 10-50
- **Trade-off**
  - @10m: 5000 operations / transmitted bit
  - @ 1m: 0.5 operations / transmitted bit

The Implementation Opportunities

System-on-a-Chip



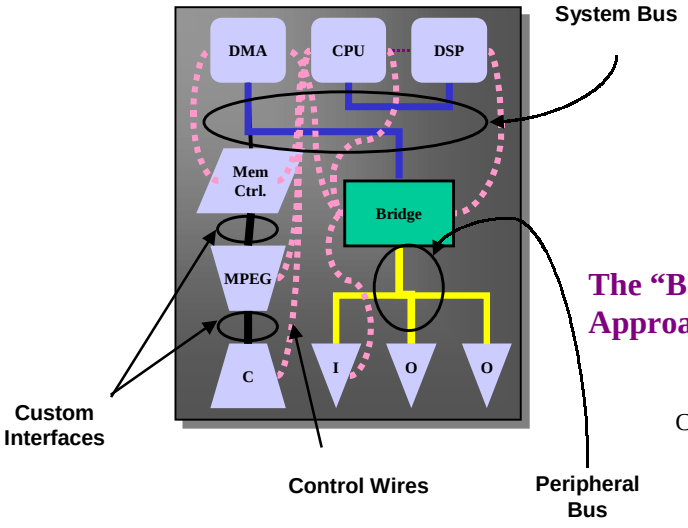
SOC anno 2010

Embedded applications where cost, performance, and energy are the real issues!
DSP and control intensive
Mixed-mode
Combines programmable and application-specific modules

The System-on-a-Chip Nightmare

"Femme se coiffant"
Pablo Ruiz Picasso
1940

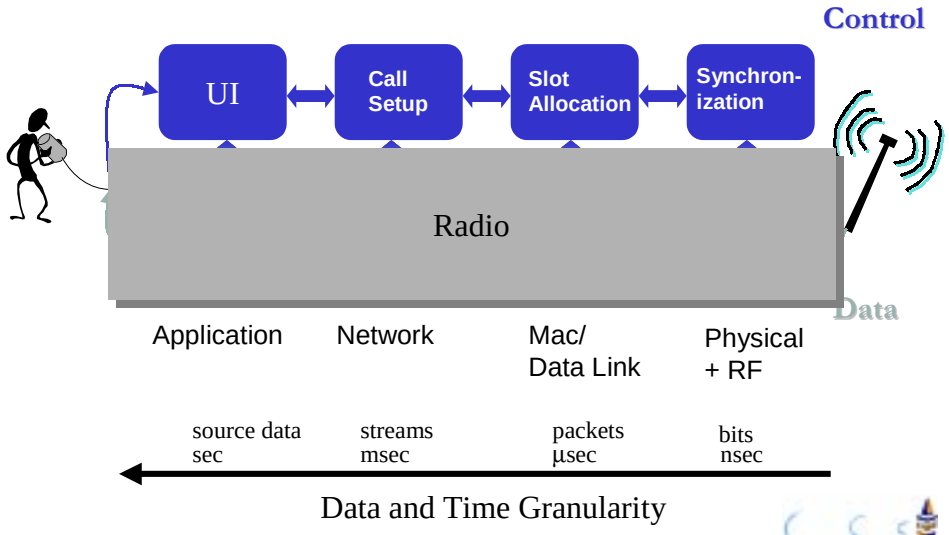
The System-on-a-Chip Nightmare



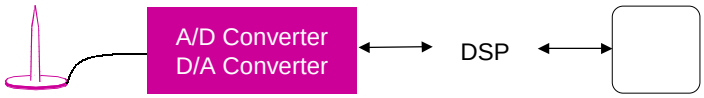
The "Board-on-a-Chip" Approach

Courtesy of Sonics, Inc

The Wireless Challenge

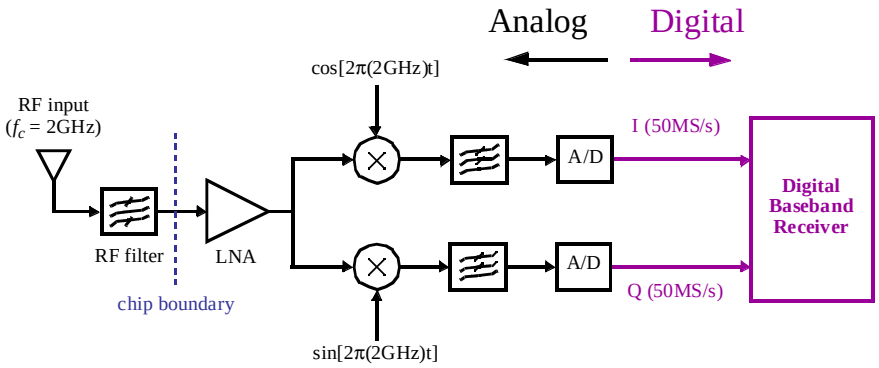


The Software Radio

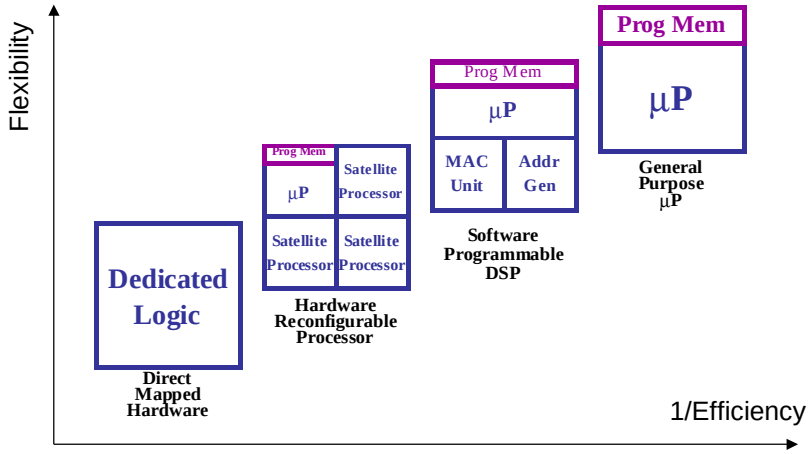


- **Idea: Digitize (wideband) signal at antenna and use signal processing to extract desired signal**
- **Leverages of advances in technology, circuit design, and signal processing**
- **Software solution enables flexibility and adaptivity, but at huge price in power and cost**
- **16 bit A/D converter at 2.2 GHz dissipates 1 to 10 W**

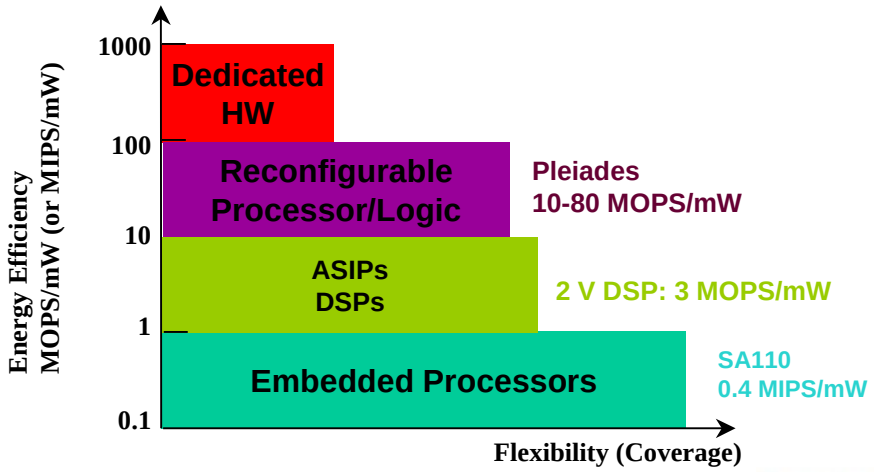
The Mostly Digital Radio



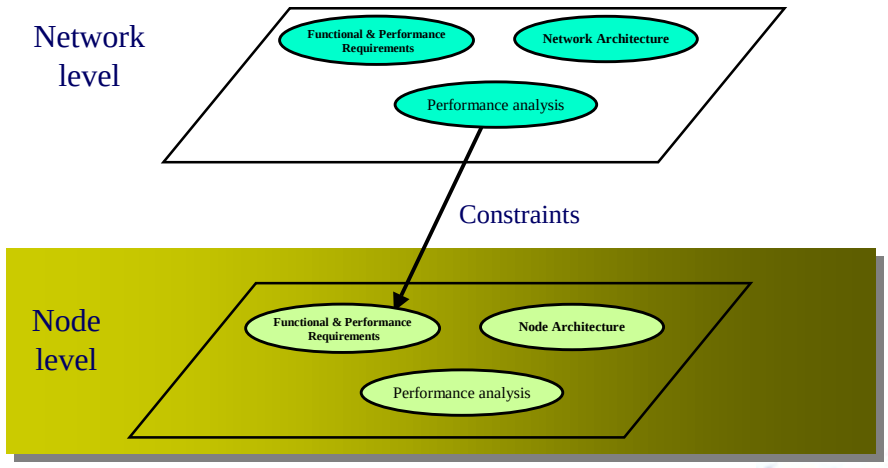
Architectural Choices



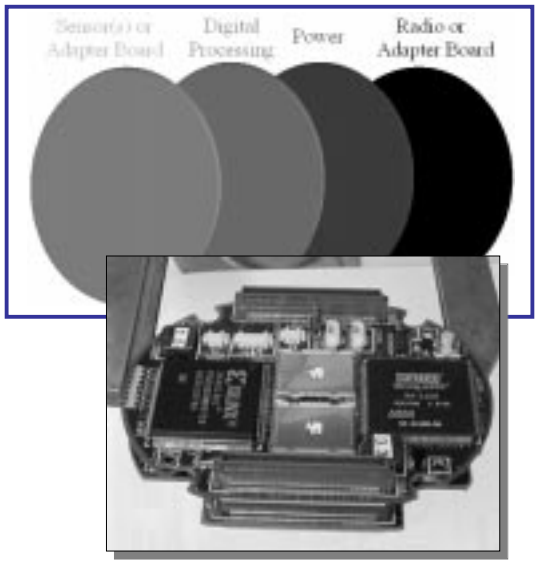
The Energy-Flexibility Gap



System Optimization Hierarchy

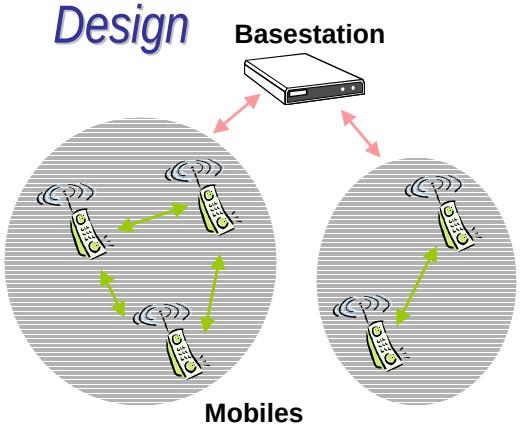


The fully programmable approach



- **Flexible platform for experimentation on networking and protocol strategies**
- **Size: 3”x4”x2”**
- **Power dissipation < 2 W (peak)**
- **Multiple radio modules: Bluetooth, Proxim, …**
- **Collection of sensor and monitor cards**
- **Fully operational by late spring (including software support system)!**

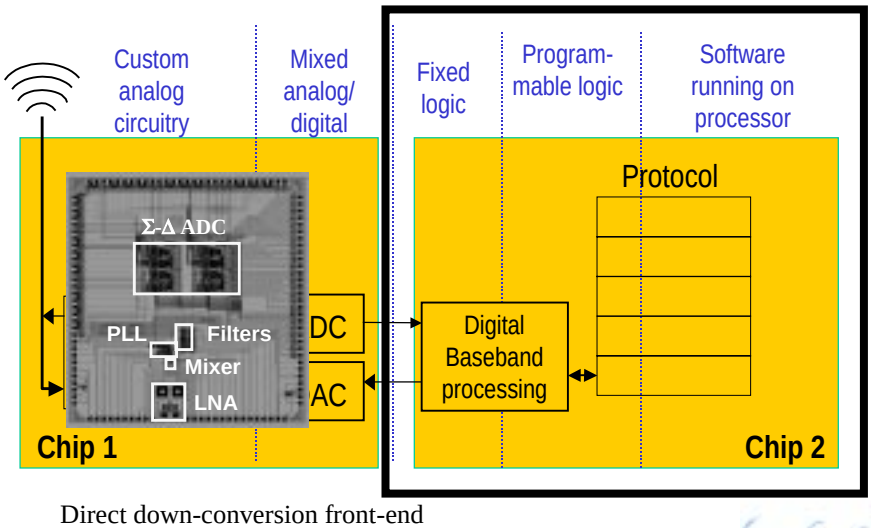
Digital Intercom — A Design Exercise in Communication/Component Based Design



Up to 20 users per cell @ 64 kbit/sec per link
TDMA selected as MAC protocol

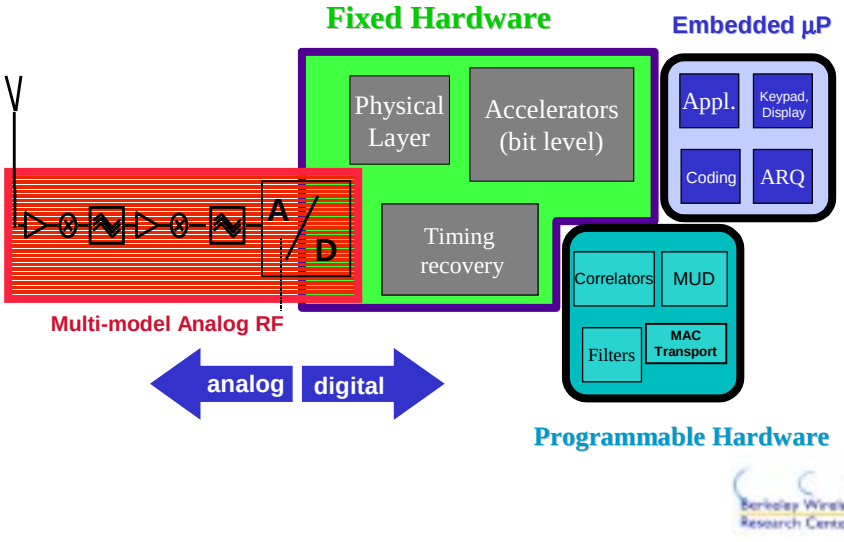
- **Known and tested specification of limited complexity allows focus on architectural implementation methodology**
- **Two-chip implementation leverages separates between analog (RF) and digital design concerns**
- **Duration of exercise: 1 year (summer ‘00)**

Two-Chip Intercom

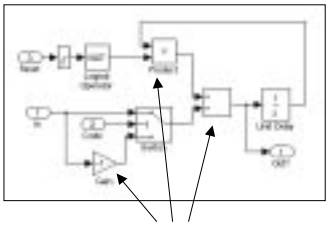


Direct down-conversion front-end
(Yee et al)

The Target Architecture

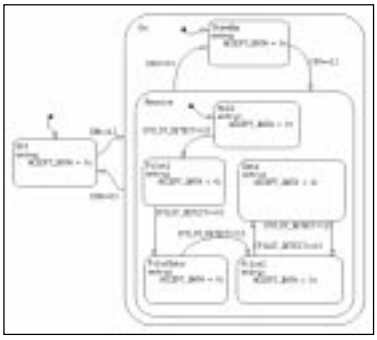


Digital Baseband



Simulink example:
Matched filter correlator

Stateflow example:
Receiver controller



Stage 1: floating point blocks
Stage 2: fixed point blocks

Design Estimations (First order):

RF + ADC/DAC

Transmit: 30 mW

Receive: 70 mW

Digital (conservative)

Transmit: 20 mW (100,000 transistors)

Receive: 80 mW (700,000 transistors)

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Physical layer timing analysis (from Simulink)

Abstracted Simulation Results Drive Protocol Design!

Estimates for the performance of the TCI Physical layer

	Rates		Duration		
	Hz	MHz	s	us	
Chip	2.50E+07	25.00	4.00E-08	0.04	
Symbol	8.06E+05	0.81	1.24E-06	1.24	
Bit	1.61E+06	1.61	6.20E-07	0.62	
				0.00	
Pilot symbol			1.24E-06	1.24	
Pilot sequence			1.86E-05	18.60	
The transmit protocol will send a pilot sequence, some small number of dummy data bits (PD), another pilot sequence, and the real data bits (DAT) with the constraint that DAT<safe # sequential symbols					
TX = PS | PD | PS | DAT					
PD			0.0000124	12.40	
DAT			0.004712	4712.00	
time from RX to TX transition until :					
first DAT clock on transmitter			4.96E-05	49.60	(1)
time from TXCLK on Radio A until:					
RXCLK on radio B			2.58E-06		
time from TX on Radio A, and RX on radio B until:					
first DAT2 RXCLK on radio B			5.22E-05	52.18	(3)

Additional Calculations

Chips per Symbol	31	
Bits per Symbol	2	
Pilot sequence length	15	
Channel coherency time	1.00E-01	
BB clock coherency time (s)	5.00E-03	
Max # sequential symbols (s)	4.03E+03	
Safety margin	95.00%	
Safe # sequential symbols	3.83E+03	
PD (# of symbols)	10	
DAT (# of symbols)	3800	OK
	meters	feet
Min distance	5	16.40
Max distance	10	32.81
		1
		1.00E+09
	s	us
	1.64E-08	0.02
	3.28E-08	0.03
Max time of flight (suggested by Paul bwo Dennis)	1.00E-07	0.10

Tool: Microsoft Excel

Radio Turn-around Time

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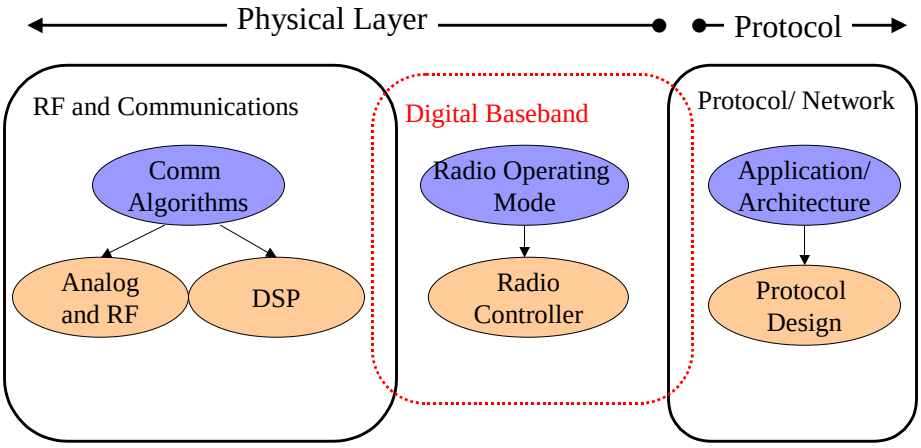
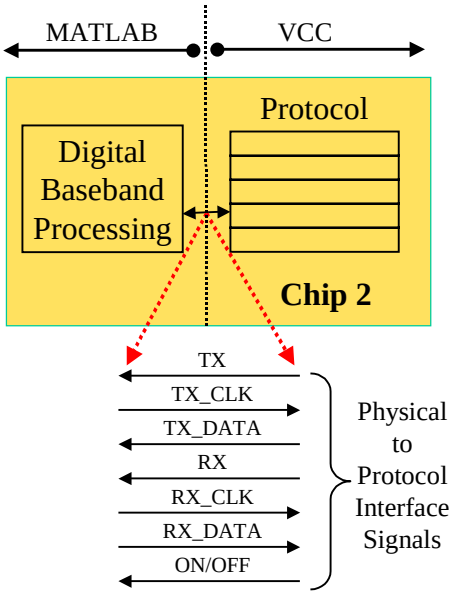
Physical Layer Design



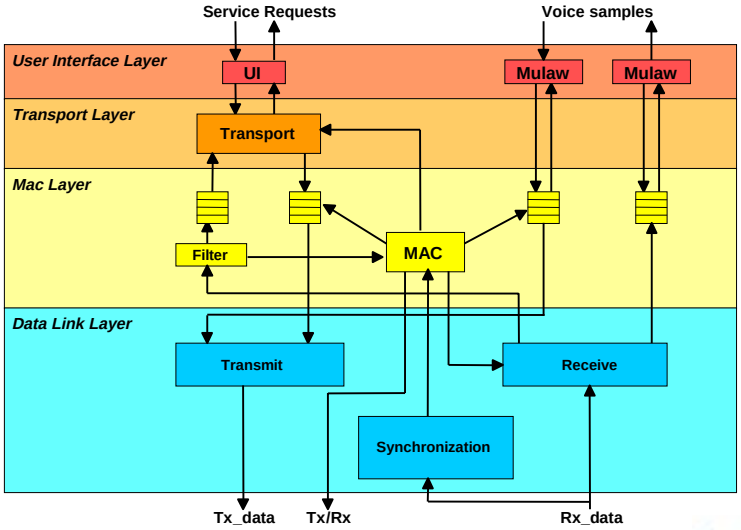
Digital baseband bridges gap between RF/Comm and protocol/network

Physical to Protocol Interface



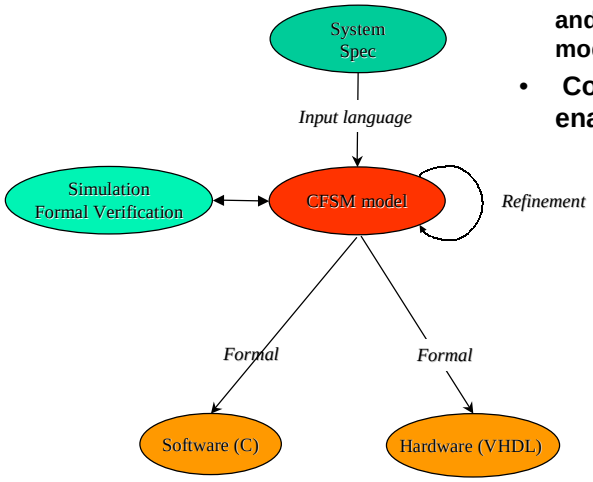
- **Different tools**
- **Verification relying on co-simulation**
- **Interface design critical to ensuring final designs work together**
  - **Define small number of interface signals**
  - **Clearly specify behavior**

The Intercom Protocol Stack



Refinement-based Protocol Design Methodology

A CFSM-based approach



Advantages

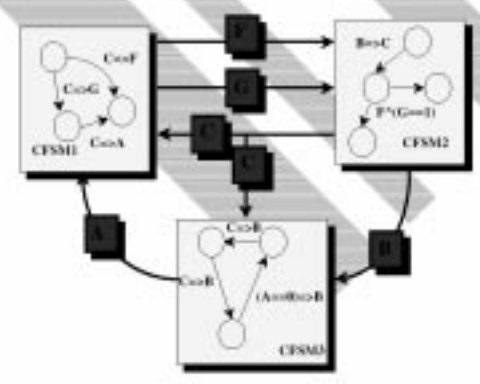
- **Combines synchronous and asynchronous models**
- **Constrained model enables verification**

Co-design Finite State machines

- **Three-level hierarchy**
  - **top level: asynchronous, partially ordered**
    (bounded buffer non- blocking single- read communication)
  - **middle level: synchronous FSM**
    (atomic event- and condition- based transition)
  - **bottom level: Synchronous DataFlow- like**
    (FSM provides tokens and selects active sub- network)

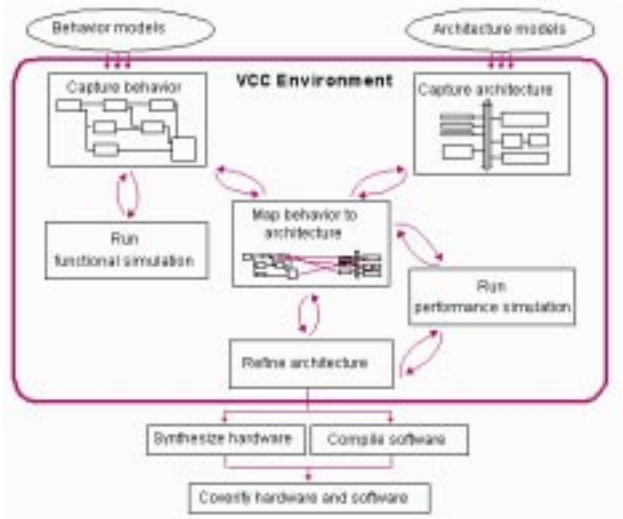
Network of CFSMs: Depth-1 Buffers

- **Globally Asynchronous, Locally Synchronous (GALS) model**



(from ee249: http://www-cad.eecs.berkeley.edu/Respep/Research/hsc/class/index.html

POLIS/VCC Design Flow



** (from the VCC manual)*

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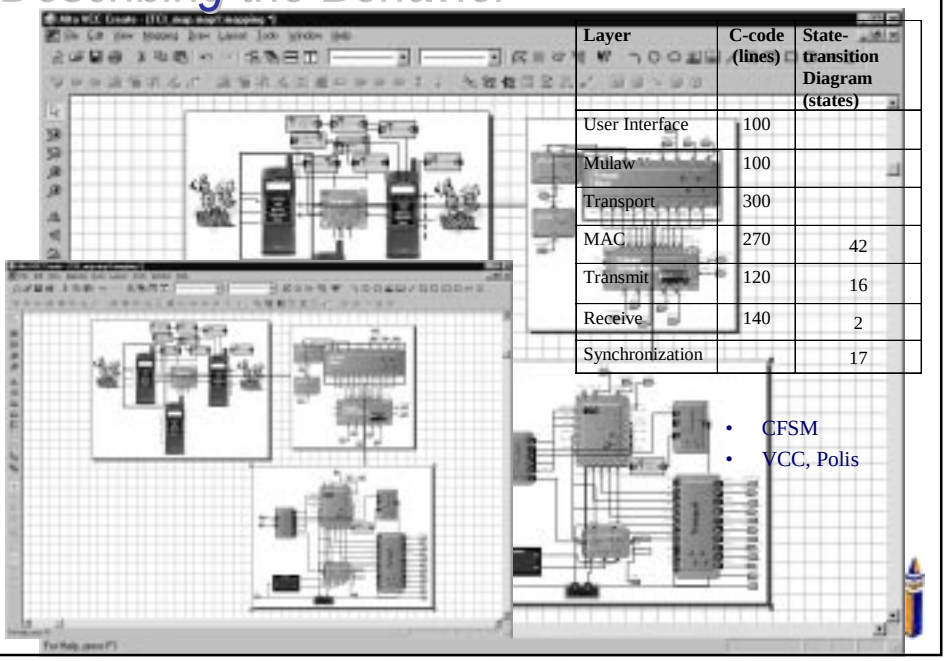
Describing the Behavior



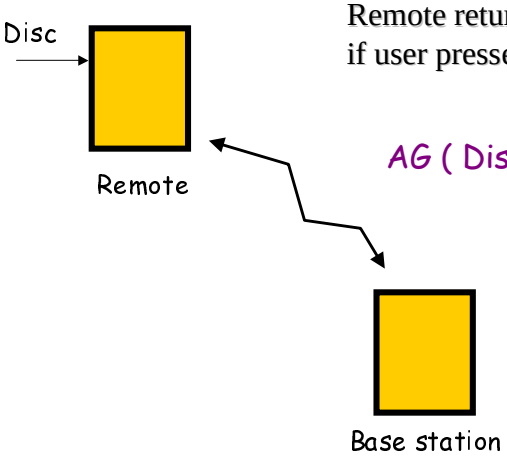
Layer	C-code (lines)	State-transition Diagram (states)
User Interface	100	
Mulaw	100	
Transport	300	
MAC	270	42
Transmit	120	16
Receive	140	2
Synchronization		17

- CFSM
- VCC, Polis

Formal Verification

- **System satisfies certain properties?**
  - System described in some formal mathematical languages (e.g. Esterel)
  - Properties written in some formal logic (e.g. LTL) or formal model (e.g. Esterel)
- **Property Verification**
  - Invariant (only one remote can send voice data in any time slot)
  - Response (if a remote sends a request to the base station, then eventually there is an acknowledgement)
  - deadlock freedom
- **Refinement Checking**
  - Does the (low-level) implementation conform with the (high-level) specification?
    (Do the mapped CFSMs function the same as the specification?)
- **Mocha (Henzinger): Modularity in Model Checking**

Example of Property Verification



Remote returns to the disconnect state if user presses the disconnect button.

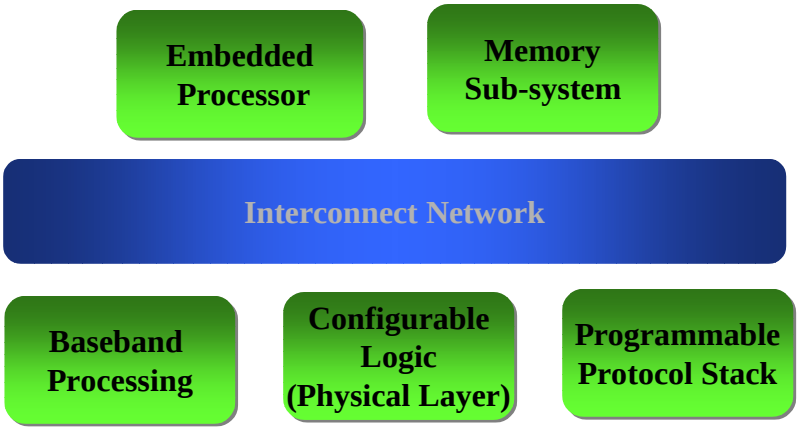
AG (Disc→ AF (Not Conn))

×NOT OK

Why it Fails?

- Remote accepts ***Disc*** from the user even if it is not connected
- After the remote has sent ***DiscReq*** and **waits** for acknowledgement
- However, base station **ignores** ***DiscReq*** if remote is not registered

Targeted Implementation Platform



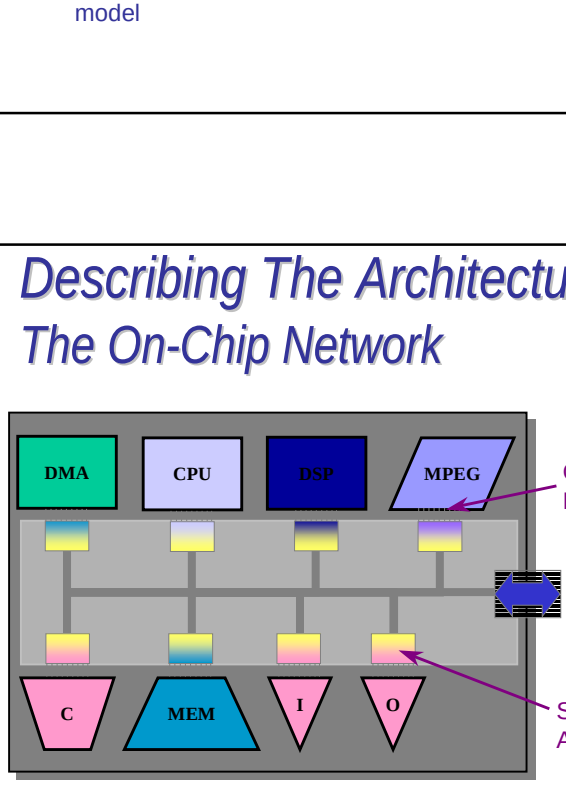
Benefit: Build library of computational and networking modules (and models)

Describing the Architecture

- **Xtensa embedded CPU (Tensilica, Inc)**
  - Configurability allows designer to keep "minimal" hardware overhead
  - ISA (compatible with 32 bit RISC) can be extended for software optimizations
  - Fully synthesizable
  - Complete HW/SW suite
- **VCC modeling for exploration**
  - Requires mapping of "fuzzy" instructions of VCC processor model to real ISA
  - Requires multiple models depending on memory configuration
  - ISS simulation to validate accuracy of model

◆ **Tensilica model in VCC**

```
inst,LD,2          inst,MUL.c,9       inst,DIV.i,118
inst,LI,1          inst,MUL.s,10      inst,DIV.l,122
inst,ST,2          inst,MUL.i,18      inst,DIV.f,145
inst,OP.c,2        inst,MUL.l,22      inst,DIV.d,155
inst,OP.s,3        inst,MUL.f,45      inst,IF,5
inst,OP.i,1        inst,MUL.d,55      inst,GOTO,2
inst,OP.l,1        inst,DIV.c,19      inst,SUB,19
inst,OP.f,1        inst,DIV.s,110     inst,RET,21
inst,OP.d,6
```



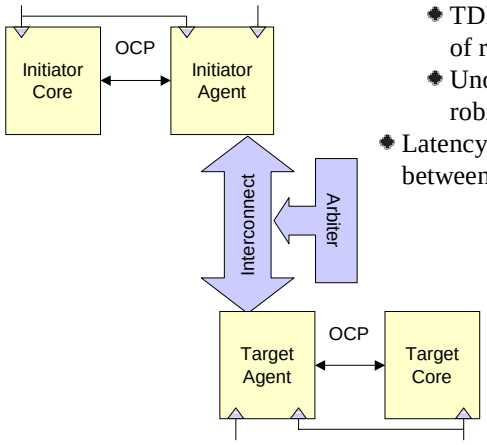
Guaranteed Bandwidth Arbitration

Example: "The Silicon Backplane" (Sonics, Inc)

Describing The Architecture
The On-Chip Network

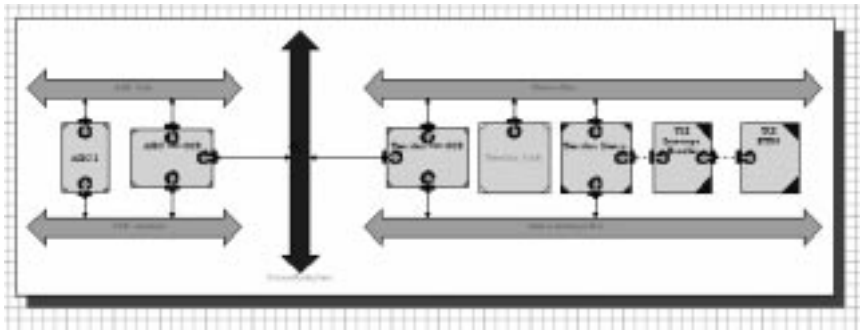
Describing the Architecture

- SONICS model in VCC



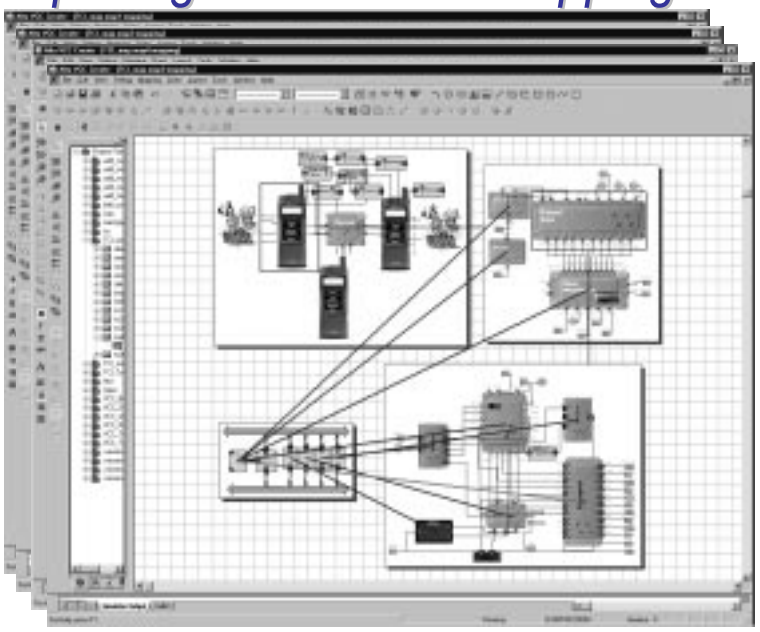
- Flexible bandwidth arbitration model
  - TDMA slot map gives slot owner right of refusal
  - Unowned/unused slots fall to round-robin arbitration
- Latency after slice granted is user-specified between 2-7 Bus Clock cycles

TCI Architecture



ASIC SiliconBackplane Tensilica Xtensa

Exploring Architectural Mappings



Software Processor

Application

Transport

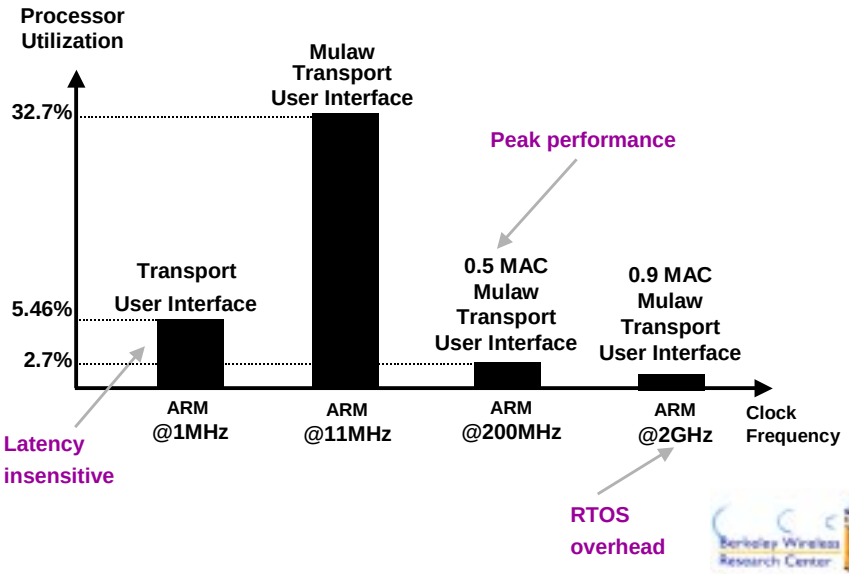
Mu-law

MAC

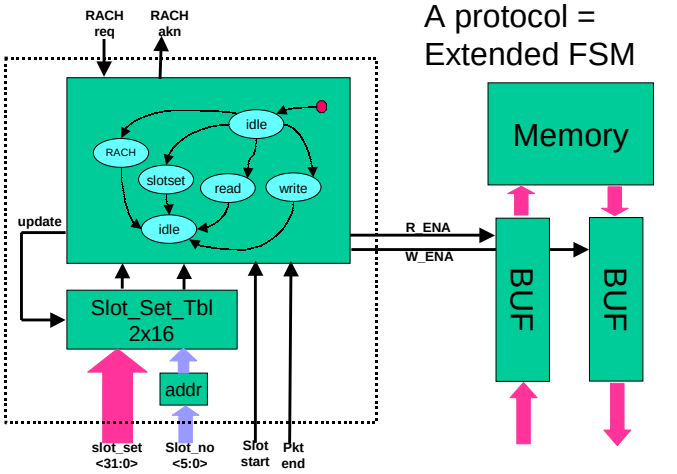
ASIC Accelerators

Rest

Processor Utilization - Estimation



Implementation Fabrics for Protocols



Intercom TDMA MAC

Intercom TDMA MAC Implementation alternatives

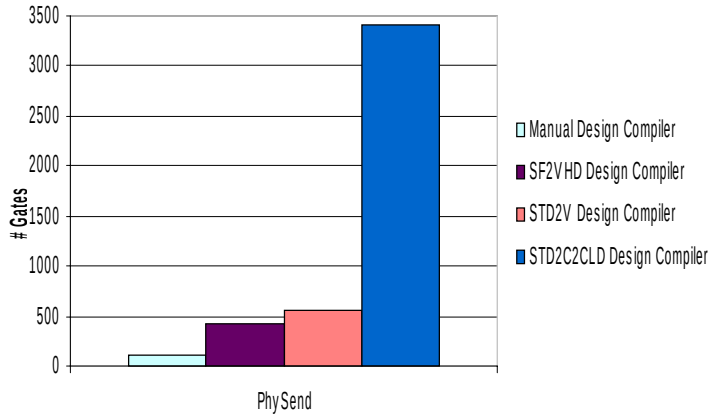
	ASIC	FPGA	ARM8
Power	0.26mW	2.1mW	*114mW*
Energy	10.2pJ/op	81.4pJ/op	*n*457pJ/op*

ASIC: 1V, 0.25 µm CMOS process
FPGA: 1.5 V 0.25 µm CMOS low-energy FPGA
ARM8: 1 V 25 MHz processor; n = 13,000
Ratio: 1 - 8 - >> 400

Idea: Exploit model of computation: concurrent finite state machines, communicating through message passing

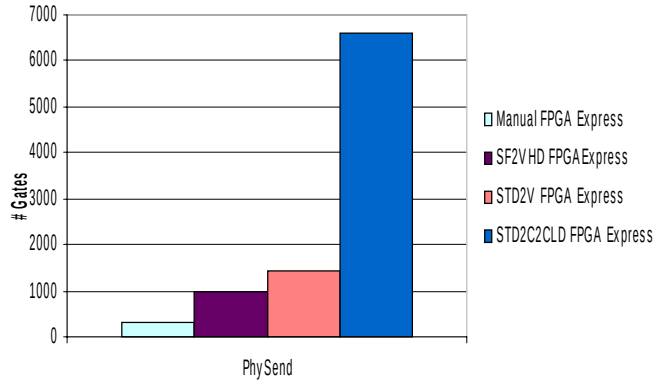
HW Mapping Experiment: STD to Std. Cell

Area Comparison – Manual versus Automated



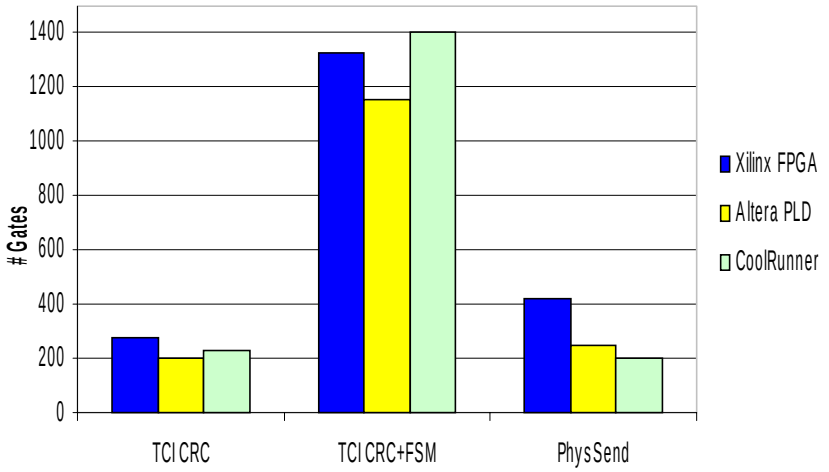
HW Mapping Experiment: STD to FPGA

Area Comparison – Manual versus Automated



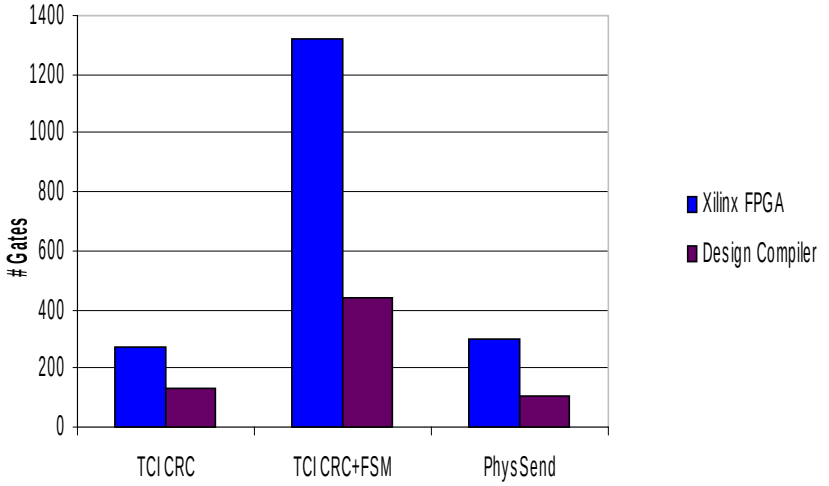
HW Mapping Experiment: STD to Flexible Imp.

Area Comparison - FPGA x PLD (Manual)



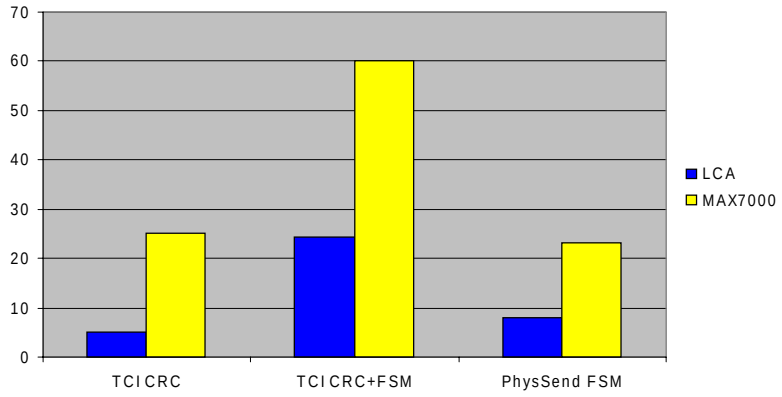
HW Mapping Experiment: Flexible versus Fixed

Area Comparison – FPGA x Std.Cell (Manual)

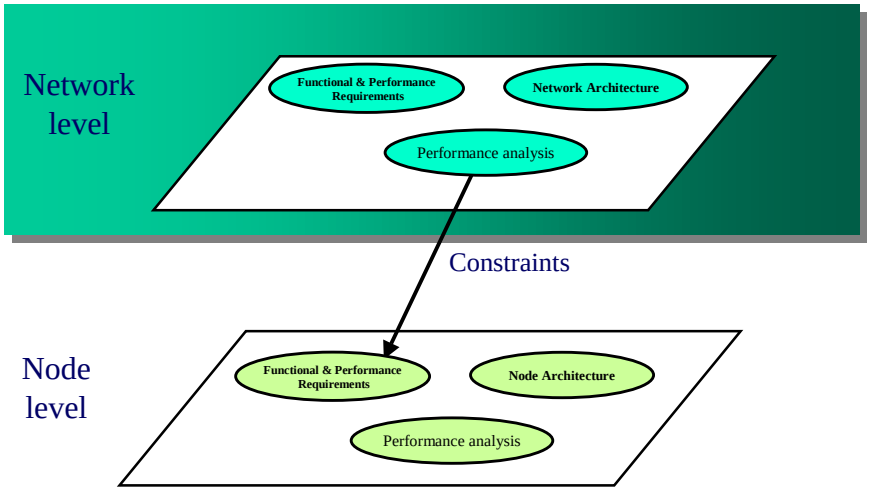


HW Mapping Experiment: Power

FPGA versus PLD



Hierarchy in System Optimization



The Applications and Specs

The Obvious Choice -The Smart Home and Network Appliances

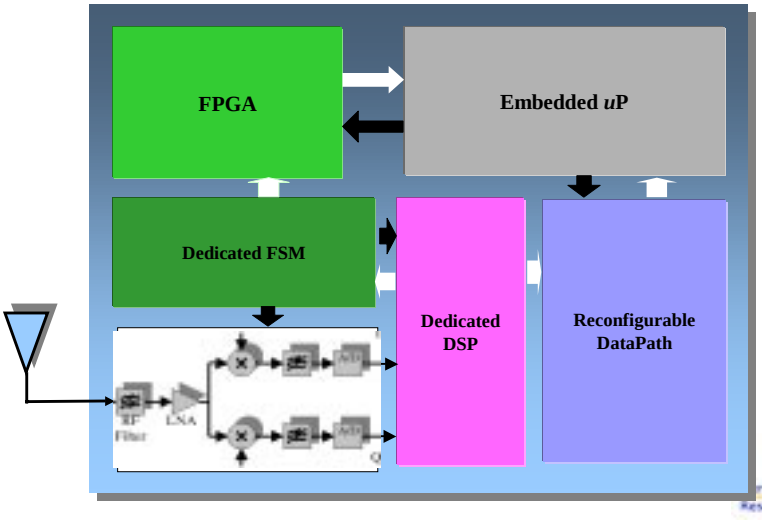
Dense network of sensor and monitor nodes

Security
Environment monitoring and control
Object tagging
Identification

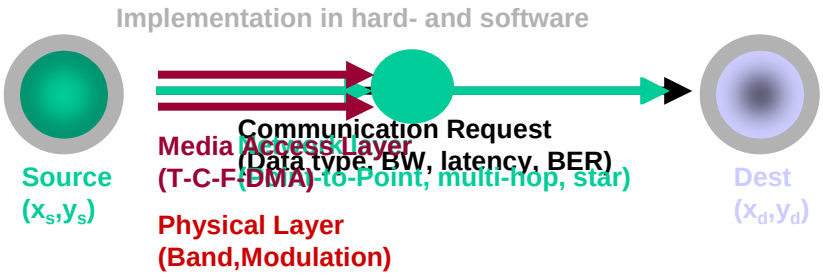
System Requirements and Constraints

- **Large numbers of nodes — between 0.05 and 1 nodes/m^2**
- **Cheap (<0.5$) and small (< 1 cm^3)**
- **Limited operation range of network — maximum 50-100 m**
- **Low data rates per node — 1-10 bits/sec average**
  - up to 10 kbit/sec in rare local connections to potentially support non-latency critical voice channel
- **Crucial Design Parameter:**
  Spatial capacity (or density) — 100-200 bits/sec/m^2

The Software-Defined Radio



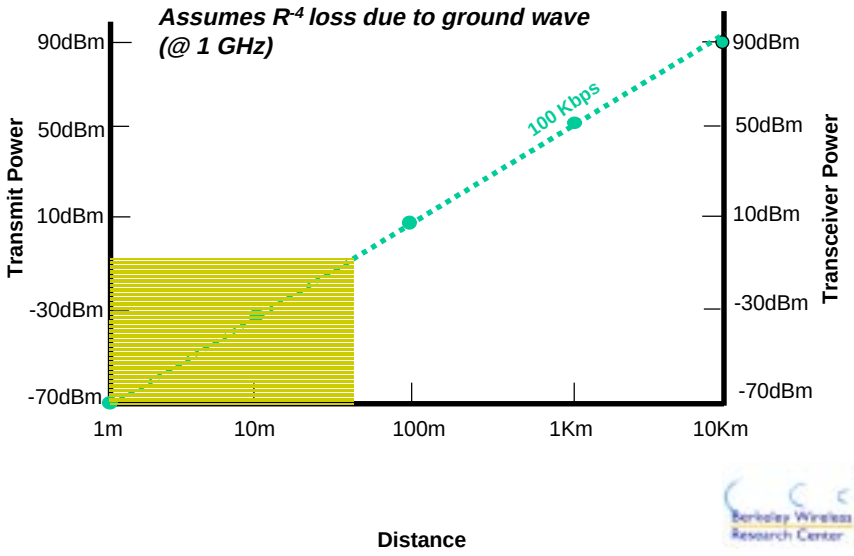
System-Level Design Space Exploration



- **Based on well-defined abstraction layers**
- **Step-wise refinement (partitioning, resource mapping and sharing) enables correctness verification**
- **Automatic synthesis of adaptive protocols in hard- and software**

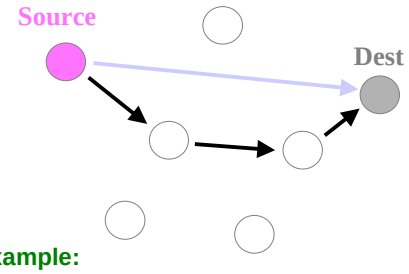
PicoRadio Energy Optimization

The Cost of Communication



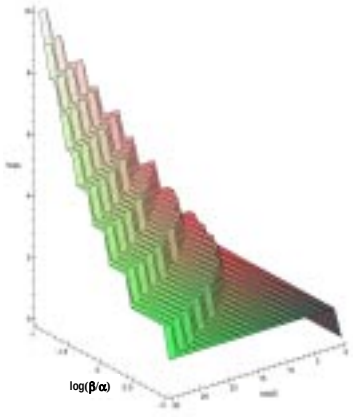
Communicating over Long Distances

Multi-hop Networks



Example:

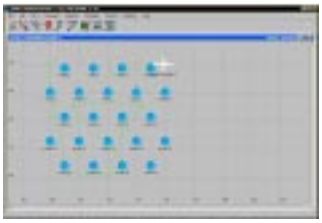
- **1 hop over 50 m**
  1.25 nJ/bit
- **5 hops of 10 m each**
  5×2 pJ/bit = 10 pJ/bit
- **Multi-hop reduces transmission energy by 125!**
  (assuming path loss exponent of 4)



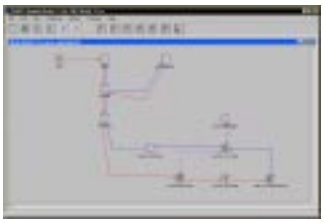
Optimal number of hops needed for free space path loss.

But … network discovery and maintenance overhead

Network Model

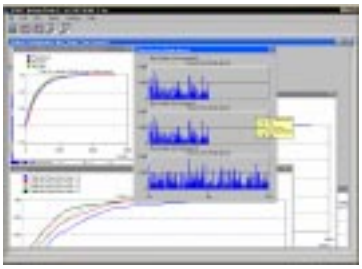


Node Model



Process Model

Analysis Viewer

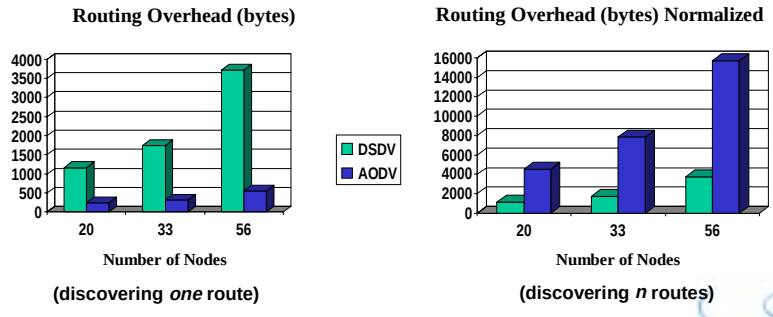


OPNET

Network Simulator

Comparing the approaches from an energy perspective

- **Energy = Eb * Packet Size**
- **Reactive Routing good for rarely used routes**
- **Proactive Routing good for frequently used routes**
- **Need solution that is more adequate for problem at hand: class-based and location-based addressing.**



Summary

- Low-energy design ascends to prime time forced mainly by the last-meter problem
- System-on-a-Chip approach enables and demands heterogeneous implementation strategies, sometimes involving non-intuitive and innovative design platforms
- Design exploration over various fabrics and partitions has dramatic impact on dominant metrics, such as energy and cost
- It requires orthogonalization of function and architecture, supplemented with performance models (cost, time, energy)
- This methodology holds at all levels of the system hierarchy