The Devices

Jan M. Rabaey
Goal of this chapter

- Present intuitive understanding of device operation
- Introduction of basic device equations
- Introduction of models for manual analysis
- Introduction of models for SPICE simulation
- Analysis of secondary and deep-sub-micron effects
- Future trends
The Diode

Cross-section of $pn$-junction in an IC process

One-dimensional representation diode symbol
Depletion Region

(a) Current flow.

(b) Charge density.

(c) Electric field.

(d) Electrostatic potential.
Diode Current

\[ I_D = I_S \left( e^{V_D/\Phi T} - 1 \right) \]

(a) On a linear scale.

(b) On a logarithmic scale (forward bias).
Forward Bias

\[ n_{p0} \]

\[ p_{n0} \]

\[ p_{n}(W_2) \]

\[ L_p \]

p-region

\[ -W_1 \]

\[ 0 \]

\[ W_2 \]

n-region

Figure: Forward Bias in a p-n junction. The diagram illustrates the carrier diffusion across the junction, with the p-region and n-region labeled accordingly. The notation \( p_{n0} \) represents the concentration of holes in the n-type region, and \( n_{p0} \) represents the concentration of electrons in the p-type region.
Reverse Bias

![Diagram showing reverse bias in a p-n diode with regions labeled p-region and n-region, and diffusion indicated by an arrow labeled "diffusion".]
Diode Types

Short-base Diode
(standard in semiconductor devices)

Long-base Diode
Models for Manual Analysis

(a) Ideal diode model

(b) First-order diode model

\[ I_D = I_S(e^{V_D/\phi T} - 1) \]
Junction Capacitance

\[ C_j = \frac{C_{j0}}{(1 - V_D l \phi_0)^m} \]

- \( m = 0.5 \): abrupt junction
- \( m = 0.33 \): linear junction
Diffusion Capacitance

\[ C_d = \frac{dQ_D}{dV_D} = \tau \frac{dI_D}{T_dV_D} \approx \frac{\tau I_D}{T_d} \phi_T \]
Diode Switching Time

\[ V_{\text{src}} (t) = \begin{cases} V_1 & \text{if } t < 0 \\ V_2 & \text{if } t \geq 0 \end{cases} \]

\[ V_D = \frac{1}{R_{\text{src}}} \int I_D (t) \, dt \]

Excess charge

Space charge

\[ V_D \]

ON

OFF

ON

Time
Secondary Effects

Avalanche Breakdown
Diode Model
## SPICE Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
<th>Default Value</th>
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</thead>
<tbody>
<tr>
<td>Saturation current</td>
<td>$I_S$</td>
<td>IS</td>
<td>A</td>
<td>1.0 E-14</td>
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<td>Emission coefficient</td>
<td>$n$</td>
<td>N</td>
<td>-</td>
<td>1</td>
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<td>Series resistance</td>
<td>$R_S$</td>
<td>RS</td>
<td>$\Omega$</td>
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<td>Transit time</td>
<td>$\tau_T$</td>
<td>TT</td>
<td>sec</td>
<td>0</td>
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<tr>
<td>Zero-bias junction capacitance</td>
<td>$C_{j0}$</td>
<td>CJ0</td>
<td>F</td>
<td>0</td>
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<tr>
<td>Grading coefficient</td>
<td>$m$</td>
<td>M</td>
<td>-</td>
<td>0.5</td>
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<tr>
<td>Junction potential</td>
<td>$\phi_0$</td>
<td>VJ</td>
<td>V</td>
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</table>

First Order SPICE diode model parameters.
The MOS Transistor

CROSS-SECTION of NMOS Transistor
Cross-Section of CMOS Technology
MOS transistors
Types and Symbols

- **NMOS Enhancement**
- **PMOS Enhancement**
- **NMOS Depletion**
- **NMOS with Bulk Contact**
Threshold Voltage: Concept
The Threshold Voltage

\[ V_T = \phi_{mS} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}} \]

- **Workfunction Difference**
- **Surface Charge**
- **Body Effect Coefficient**
- **Implants**

\[ V_T = V_{TO} + \gamma \left( \sqrt{-2\phi_F + V_{SB}} - \sqrt{-2\phi_F} \right) \]

with

\[ V_{TO} = \phi_{mS} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}} \]

and

\[ \gamma = \frac{2qe_{s_i}N_A}{C_{ox}} \]
Current-Voltage Relations

MOS transistor and its bias conditions
Current-Voltage Relations

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

$$I_D = \frac{k'_n W}{2} \left( V_{GS} - V_T \right)^2 (1 + \lambda V_{DS})$$

Channel Length Modulation
Transistor in Saturation

\[ V_{DS} > V_{GS} - V_T \]

Diagram showing the saturation region of a transistor with labels for source (S), gate (G), drain (D), and n+ regions.
I-V Relation

NMOS Enhancement Transistor: $W = 100 \ \mu m$, $L = 20 \ \mu m$
A model for manual analysis

\[ V_{DS} \geq V_{GS} - V_T \]

\[ I_D = \frac{\kappa' n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

\[ V_{DS} < V_{GS} - V_T \]

\[ I_D = \kappa' n \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \]

with

\[ V_T = V_{T0} + \gamma (\sqrt{2\phi_F + V_{SB}} - \sqrt{-2\phi_F}) \]
Dynamic Behavior of MOS Transistor
The Gate Capacitance

(a) Top view.

(b) Cross-section

\[ C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL \]
Average Gate Capacitance

Different distributions of gate capacitance for varying operating conditions

<table>
<thead>
<tr>
<th>Operation Region</th>
<th>$C_{gb}$</th>
<th>$C_{gs}$</th>
<th>$C_{gd}$</th>
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</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>$C_{ox} W_{L_{eff}}$</td>
<td>0</td>
<td>0</td>
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<tr>
<td>Triode</td>
<td>0</td>
<td>$C_{ox} W_{L_{eff}}/2$</td>
<td>$C_{ox} W_{L_{eff}}/2$</td>
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<tr>
<td>Saturation</td>
<td>0</td>
<td>$(2/3)C_{ox} W_{L_{eff}}$</td>
<td>0</td>
</tr>
</tbody>
</table>

Most important regions in digital design: saturation and cut-off
Diffusion Capacitance

\[ C_{\text{diff}} = C_{\text{bottom}} + C_{\text{sw}} = C_j \times \text{AREA} + C_{jsw} \times \text{PERIMETER} \]

\[ = C_j L_s W + C_{jsw} (2L_s + W) \]
Junction Capacitance

\[ C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m} \]
Linearizing the Junction Capacitance

Replace non-linear capacitance by large-signal equivalent linear capacitance which displaces equal charge over voltage swing of interest

\[ C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0} \]

\[ K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1 - m)} \left[ (\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m} \right] \]
The Sub-Micron MOS Transistor

• Threshold Variations
• Parasitic Resistances
• Velocity Saturation and Mobility Degradation
• Subthreshold Conduction
• Latchup
Threshold Variations

Threshold as a function of the length (for low $V_{DS}$)

Drain-induced barrier lowering (for low $L$)

Long-channel threshold

Low $V_{DS}$ threshold
Parasitic Resistances

\[ V_{GS,\text{eff}} \]

\[ S \quad R_S \quad G \quad D \quad R_D \]

Polysilicon gate

Drain contact

Drain

\[ L_D \]

\[ W \]
Velocity Saturation (1)

(a) Velocity saturation

\( \nu_{sat} = 10^7 \)

Constant mobility (slope = \( \mu \))

\( E_{sat} = 1.5 \)

\( E \) (V/\( \mu \)m)

\( \nu_n \) (cm/sec)

(b) Mobility degradation

\( \mu_{n0} \)

\( E_t \) (V/\( \mu \)m)

\( \mu_n \) (cm²/Vs)

Constant velocity
Velocity Saturation (2)

(a) $I_D$ as a function of $V_{DS}$

(b) $I_D$ as a function of $V_{GS}$ (for $V_{DS} = 5$ V).

Linear Dependence on $V_{GS}$
Sub-Threshold Conduction

\[ \ln(I_D) (\text{A}) \]

\[ V_{GS} (V) \]

Linear region

Subthreshold exponential region

\[ V_T \]
Latchup

(a) Origin of latchup

(b) Equivalent circuit

\( V_{DD} \)

\( R_{nwell} \)

\( n-source \)

\( p-source \)

\( R_{psubs} \)

\( p-substrate \)
SPICE MODELS

Level 1: Long Channel Equations - Very Simple

Level 2: Physical Model - Includes Velocity Saturation and Threshold Variations

Level 3: Semi-Emperical - Based on curve fitting to measured devices

Level 4 (BSIM): Emperical - Simple and Popular
### MAIN MOS SPICE PARAMETERS

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
<th>Default Value</th>
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<tr>
<td>SPICE Model Index</td>
<td>LEVEL</td>
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<tr>
<td>Zero-Bias Threshold Voltage</td>
<td>VT0</td>
<td>VT0</td>
<td>V</td>
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<td>Process Transconductance</td>
<td>h'</td>
<td>KP</td>
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<td>Body-Bias Parameter</td>
<td>γ</td>
<td>GAMMA</td>
<td>V/0.5</td>
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<td>Channel Modulation</td>
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<td>LAMBDA</td>
<td>1/V</td>
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<td>Oxide Thickness</td>
<td>tox</td>
<td>TOX</td>
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<td>Lateral Diffusion</td>
<td>xd</td>
<td>LD</td>
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<td>Metallurgical Junction Depth</td>
<td>xj</td>
<td>XJ</td>
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<td>Surface Inversion Potential</td>
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<td>PHI</td>
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<td>Substrate Doping</td>
<td>NA,ND</td>
<td>NSUB</td>
<td>cm-3</td>
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<td>Surface State Density</td>
<td>Qss/q</td>
<td>NSS</td>
<td>cm-3</td>
<td>0</td>
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<tr>
<td>Fast Surface State Density</td>
<td>NFS</td>
<td></td>
<td>cm-3</td>
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<tr>
<td>Total Channel Charge Coefficient</td>
<td>NEFF</td>
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<tr>
<td>Type of Gate Material</td>
<td>TPG</td>
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<td>Surface Mobility</td>
<td>m0</td>
<td>U0</td>
<td>cm2/V-sec</td>
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<td>VMAX</td>
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<td>Mobility Critical Field</td>
<td>xcrit</td>
<td>UCRIT</td>
<td>V/cm</td>
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<td>Critical Field Exponent in Mobility Degradation</td>
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<td>Transverse Field Exponent (mobility)</td>
<td>UTRA</td>
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# SPICE Parameters for Parasitics

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<tbody>
<tr>
<td>Source resistance</td>
<td>$R_S$</td>
<td>RS</td>
<td>Ω</td>
<td>0</td>
</tr>
<tr>
<td>Drain resistance</td>
<td>$R_D$</td>
<td>RD</td>
<td>Ω</td>
<td>0</td>
</tr>
<tr>
<td>Sheet resistance (Source/Drain)</td>
<td>$R_o$</td>
<td>R.SH</td>
<td>Ω/$\Omega$</td>
<td>0</td>
</tr>
<tr>
<td>Zero Bias Bulk Junction Cap</td>
<td>$C_{j0}$</td>
<td>CJ</td>
<td>F/m$^2$</td>
<td>0</td>
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<tr>
<td>Bulk Junction Grading Coeff.</td>
<td>$m$</td>
<td>MJ</td>
<td>-</td>
<td>0.5</td>
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<tr>
<td>Zero Bias Side Wall Junction Cap</td>
<td>$C_{jsw0}$</td>
<td>CJSW</td>
<td>F/m</td>
<td>0</td>
</tr>
<tr>
<td>Side Wall Grading Coeff.</td>
<td>$m_{sw}$</td>
<td>MJSW</td>
<td>-</td>
<td>0.3</td>
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<tr>
<td>Gate-Bulk Overlap Capacitance</td>
<td>$C_{gb0}$</td>
<td>CGBO</td>
<td>F/m</td>
<td>0</td>
</tr>
<tr>
<td>Gate-Source Overlap Capacitance</td>
<td>$C_{gs0}$</td>
<td>CGSO</td>
<td>F/m</td>
<td>0</td>
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<tr>
<td>Gate-Drain Overlap Capacitance</td>
<td>$C_{gd0}$</td>
<td>CGDO</td>
<td>F/m</td>
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<td>Bulk Junction Leakage Current</td>
<td>$I_S$</td>
<td>IS</td>
<td>A</td>
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<td>Bulk Junction Leakage Current Density</td>
<td>$J_S$</td>
<td>JS</td>
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<td>PB</td>
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## SPICE Transistors Parameters

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<td>Drawn Length</td>
<td>L</td>
<td>L</td>
<td>m</td>
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<td>Effective Width</td>
<td>W</td>
<td>W</td>
<td>m</td>
<td>-</td>
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<tr>
<td>Source Area</td>
<td>AREA</td>
<td>AS</td>
<td>m²</td>
<td>0</td>
</tr>
<tr>
<td>Drain Area</td>
<td>AREA</td>
<td>AD</td>
<td>m²</td>
<td>0</td>
</tr>
<tr>
<td>Source Perimeter</td>
<td>PERIM</td>
<td>PS</td>
<td>m</td>
<td>0</td>
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<tr>
<td>Drain Perimeter</td>
<td>PERIM</td>
<td>PD</td>
<td>m</td>
<td>0</td>
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<tr>
<td>Squares of Source Diffusion</td>
<td>NRS</td>
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<td>1</td>
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<tr>
<td>Squares of Drain Diffusion</td>
<td>NRD</td>
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Fitting level-1 model for manual analysis

Select $k'$ and $\lambda$ such that best matching is obtained @ $V_{gs} = V_{ds} = V_{DD}$
## Technology Evolution

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<tr>
<td>Channel length (μm)</td>
<td>0.4</td>
<td>0.3</td>
<td>0.25</td>
<td>0.18</td>
<td>0.13</td>
<td>0.1</td>
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<td>Gate oxide (nm)</td>
<td>12</td>
<td>7</td>
<td>6</td>
<td>4.5</td>
<td>4</td>
<td>4</td>
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<tr>
<td>$V_{DD}$ (V)</td>
<td>3.3</td>
<td>2.2</td>
<td>2.2</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>$V_T$ (V)</td>
<td>0.7</td>
<td>0.7</td>
<td>0.7</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
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<tr>
<td>NMOS $I_{D_{sat}}$ (mA/μm) ($@ V_{GS} = V_{DD}$)</td>
<td>0.35</td>
<td>0.27</td>
<td>0.31</td>
<td>0.21</td>
<td>0.29</td>
<td>0.33</td>
</tr>
<tr>
<td>PMOS $I_{D_{sat}}$ (mA/μm) ($@ V_{GS} = V_{DD}$)</td>
<td>0.16</td>
<td>0.11</td>
<td>0.14</td>
<td>0.09</td>
<td>0.13</td>
<td>0.16</td>
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</table>
Bipolar Transistor

(a) Cross-sectional view.

(b) Idealized transistor structure.
Schematic Symbols and Sign Conventions

(a) npn

(b) pnp
# Operations Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>Emitter Junction</th>
<th>Collector Junction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cut-off</td>
<td>Reverse</td>
<td>Reverse</td>
</tr>
<tr>
<td>Forward-active</td>
<td>Forward</td>
<td>Reverse</td>
</tr>
<tr>
<td>Reverse-active</td>
<td>Reverse</td>
<td>Forward</td>
</tr>
<tr>
<td>Saturation</td>
<td>Forward</td>
<td>Forward</td>
</tr>
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</table>
Forward Active Operation
Current Components

$E$, $B$, $C$

$I_E$, $I_B$, $I_C$

1, 2, 3

electrons
holes
Reverse Active
Saturation Mode

Carrier Concentration

\( n_b(0) \)
\( n_b(W) \)
\( Q_A \)
\( Q_S \)
\( n_{b0} \)

\( x \)
\( W_B \)

\( E \)
\( B \)
\( C \)

\( p_{e0} \)

\( p_{c0} \)
Cutoff

Carrier Concentration

$E$ $B$ $C$

$p_{e0}$

$n_b(0)$ $n_{b0}$ $n_b(W)$

$x$

$W_B$
Bipolar Transistor Operation

Reverse Operation

Forward Operation

Active

Saturation

$V_{CE} (V)$

$I_C (mA)$

$I_B = 25 \mu A$

$I_B = 50 \mu A$

$I_B = 75 \mu A$

$I_B = 100 \mu A$
A Model for Manual Analysis

\[ I_B = I_S \left( e^{\frac{V_{BE} \phi}{T}} - 1 \right) \]

(a) Forward-active

\[ V_{BE(on)} \]

(b) Forward-active (simplified)

\[ V_{BE(sat)} < \beta_f I_B \]

(c) Forward-saturation
Capacitive Model for Bipolar Transistor

- $Q_R$
- $Q_F$
- $C_{bc}$
- $C_{be}$
- $C_{cs}$

- Collector-substrate junction capacitance
- Base-emitter junction capacitances
- Base-collector junction capacitances
- Base charge
Junction Capacitances

\[ C_{eq} = K_{eq} C_{j0} \]

\[ K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)}[(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}] \]
Base Charge - Diffusion Capacitance

\[ I_C = \frac{Q_F}{\tau_F} \quad \text{with} \quad \tau_F = \frac{W_B^2}{2 D_B} \]

Equivalent Diffusion Capacitance

\[ C_d = \frac{I_C}{\tau_F \Phi_T} \]
Bipolar Transistors - Secondary Effects

- Early Voltage
- Parasitic Resistances
- Beta Variations
Early Voltage

Saturation

Forward
Active

$I_C$

$V_{BE1}$

$V_{BE2}$

$V_{BE3}$

$V_{CE}$

$V_A$
Parasitic Resistance

Diagram showing the parasitic resistance components:

- **n-epitaxy**
- **p-substrate**
- **n⁺ buried layer**
- **p⁺ isolation**
- **rₑ**, **rₐ**, **rₐ₂**, **rₐ₃**

The diagram illustrates the parasitic resistance network in a semiconductor device, with various resistance components labeled for analysis.
Beta Variations

\[ \ln(I) \]

\( I_{KF} \)

\( I_B \)

\( I_C \)

\( \beta_F \)

Recombination

High Level Injection

\( V_{BE} \) (linear)
SPICE models for Bipolar

\[ I_C = I_S \left( e^{\frac{V_{BE}/(n_F \Phi T)}{V_A}} - e^{\frac{V_{BC}/(n_R \Phi T)}{V_A}} \right) \left( 1 - \frac{V_{BC}}{V_A} \right) - \frac{I_S}{V_R} e^{\frac{V_{BC}/(n_R \Phi T)}{V_A}} - 1 \]

\[ I_B = \frac{I_S}{V_F} \left( e^{\frac{V_{BE}/(n_F \Phi T)}{V_A}} - 1 \right) + \frac{I_S}{V_R} e^{\frac{V_{BC}/(n_R \Phi T)}{V_A}} - 1 \]
Main Bipolar Transistor SPICE Models

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transport Saturation Current</td>
<td>$I_S$</td>
<td>IS</td>
<td>A</td>
<td>1.0E–16</td>
</tr>
<tr>
<td>Maximum Forward Current Gain</td>
<td>$\beta_F$</td>
<td>BF</td>
<td>–</td>
<td>100</td>
</tr>
<tr>
<td>Forward Current-Emission Coefficient</td>
<td>$n_F$</td>
<td>NF</td>
<td>–</td>
<td>1</td>
</tr>
<tr>
<td>Forward Early Voltage</td>
<td>$V_{AF}$</td>
<td>VAF</td>
<td>V</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Maximum Reverse Current Gain</td>
<td>$\beta_R$</td>
<td>BR</td>
<td>–</td>
<td>1</td>
</tr>
<tr>
<td>Reverse Current-Emission Coefficient</td>
<td>$n_R$</td>
<td>NR</td>
<td>–</td>
<td>1</td>
</tr>
<tr>
<td>Reverse Early Voltage</td>
<td>$V_{AR}$</td>
<td>VAR</td>
<td>V</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Corner for Forward Beta High Current Roll-off</td>
<td>$I_{KF}$</td>
<td>IKF</td>
<td>A</td>
<td>$\infty$</td>
</tr>
<tr>
<td>$be$ Junction Leakage Saturation Current</td>
<td>ISE</td>
<td>A</td>
<td>1.0E–13</td>
<td></td>
</tr>
<tr>
<td>$be$ Junction Leakage Emission Coeff.</td>
<td>NE</td>
<td>–</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>(low-current condition)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Corner for Reverse Beta High Current Roll-off</td>
<td>$I_{KR}$</td>
<td>IKR</td>
<td>A</td>
<td>$\infty$</td>
</tr>
<tr>
<td>$bc$ junction leakage saturation current</td>
<td>ISC</td>
<td>A</td>
<td>1.0E–13</td>
<td></td>
</tr>
<tr>
<td>$bc$ junction leakage emission coeff.</td>
<td>NC</td>
<td>–</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>(low-current condition)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ideal Forward Transit Time</td>
<td>$\tau_F$</td>
<td>TF</td>
<td>sec</td>
<td>0</td>
</tr>
<tr>
<td>Ideal Reverse Transit Time</td>
<td>$\tau_R$</td>
<td>TR</td>
<td>sec</td>
<td>0</td>
</tr>
</tbody>
</table>

a. Gummel-Poon Model Parameter
# Spice Parameters for Parasitics

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter Resistance</td>
<td>$r_E$</td>
<td>RE$\text{$}$</td>
<td>$\Omega$</td>
<td>0$\text{$}$</td>
</tr>
<tr>
<td>Collector Resistance</td>
<td>$r_C$</td>
<td>RC$\text{$}$</td>
<td>$\Omega$</td>
<td>0$\text{$}$</td>
</tr>
<tr>
<td>Zero-Bias Base Resistance</td>
<td>$r_{bb}$</td>
<td>RB$\text{$}$</td>
<td>$\Omega$</td>
<td>0$\text{$}$</td>
</tr>
<tr>
<td>Minimum Base Resistance</td>
<td>$\gamma$</td>
<td>RBM$\text{$}$</td>
<td>$\Omega$</td>
<td>RB$\text{$}$</td>
</tr>
<tr>
<td>Current where RB falls halfway to RBM$\text{$}$</td>
<td>$\gamma$</td>
<td>IRB$\text{$}$</td>
<td>A$\text{$}$</td>
<td>$\infty$</td>
</tr>
<tr>
<td>Zero-Bias be-Junction Capacitance</td>
<td>$C_{be0}$</td>
<td>CJE$\text{$}$</td>
<td>F$\text{$}$</td>
<td>0$\text{$}$</td>
</tr>
<tr>
<td>be-Junction Grading Coeff.</td>
<td>$m_{be}$</td>
<td>MJE$\text{$}$</td>
<td>–$\text{$}$</td>
<td>0.33$\text{$}$</td>
</tr>
<tr>
<td>be-Junction Built-in Voltage</td>
<td>$\phi_{be}$</td>
<td>VJE$\text{$}$</td>
<td>V$\text{$}$</td>
<td>0.75$\text{$}$</td>
</tr>
<tr>
<td>Zero-Bias bc-Junction Capacitance</td>
<td>$C_{be0}$</td>
<td>CJC$\text{$}$</td>
<td>F$\text{$}$</td>
<td>0$\text{$}$</td>
</tr>
<tr>
<td>bc-Junction Grading Coeff.</td>
<td>$m_{be}$</td>
<td>MJC$\text{$}$</td>
<td>–$\text{$}$</td>
<td>0.33$\text{$}$</td>
</tr>
<tr>
<td>bc-Junction Built-in Voltage</td>
<td>$\phi_{be}$</td>
<td>VJC$\text{$}$</td>
<td>V$\text{$}$</td>
<td>0.75$\text{$}$</td>
</tr>
<tr>
<td>Zero-Bias Collector-Substrate Cap.$\text{$}$</td>
<td>$C_{cso}$</td>
<td>CJS$\text{$}$</td>
<td>F$\text{$}$</td>
<td>0$\text{$}$</td>
</tr>
<tr>
<td>cs-Junction Grading Coeff.$\text{$}$</td>
<td>$m_{cs}$</td>
<td>MJS$\text{$}$</td>
<td>–$\text{$}$</td>
<td>0$\text{$}$</td>
</tr>
<tr>
<td>cs-Junction Built-in Voltage$\text{$}$</td>
<td>$\phi_{cs}$</td>
<td>VJS$\text{$}$</td>
<td>V$\text{$}$</td>
<td>0.75$\text{$}$</td>
</tr>
</tbody>
</table>
SPICE Transistor Parameters

Example transistor instantiation:

Q1 2 1 0 NPN
Q2 2 1 0 5 NPN 4

C B E S 4 transistors in parallel

Example model:

* SPICE Model for 2 x 3.75 npn transistor

.MODEL BF=100 BR=1 IS=1.E-17 VAF=50
+ TF=10E-12 TR=5E-9 IKF=2E-2 IKR=0.5
+ RE=20 RC=75 RB=120
+ CJE=20E-15 VJE=0.8 MJE=0.5 CJC=22E-15 VJC=0.7 MJC=0.33
+ CJS=47E-15 VJS=0.7 MJS=0.33
Devices parameters vary between runs and even on the same die!

Variations in the process parameters, such as impurity concentration densities, oxide thicknesses, and diffusion depths. These are caused by non-uniform conditions during the deposition and/or the diffusion of the impurities. This introduces variations in the sheet resistances and transistor parameters such as the threshold voltage.

Variations in the dimensions of the devices, mainly resulting from the limited resolution of the photolithographic process. This causes \((W/L)\) variations in MOS transistors and mismatches in the emitter areas of bipolar devices.
Impact of Device Variations

Delay of Adder circuit as a function of variations in $L$ and $V_T$