THE INVERTERS
DIGITAL GATES
Fundamental Parameters

- Functionality
- Reliability, Robustness
- Area
- Performance
  » Speed (delay)
  » Power Consumption
  » Energy
Noise in Digital Integrated Circuits

(a) Inductive coupling  

(b) Capacitive coupling  

(c) Power and ground noise
DC Operation: Voltage Transfer Characteristic

Nominal Voltage Levels

Switching Threshold

V(y) = V(x)
Mapping between analog and digital signals

- "1"
  - \(V_{OH}\)
  - \(V_{IH}\)
  - Undefined Region

- "0"
  - \(V_{IL}\)
  - \(V_{OL}\)

Graph:
- \(V(x)\) vs \(V(y)\)
- \(V_{OH}\)
- \(V_{OL}\)
- \(V_{IL}\)
- \(V_{IH}\)
- Slope = -1

Graph shows the mapping of analog and digital signals with specific voltage levels.
Definition of Noise Margins

Noise Margin High

Noise Margin Low

Gate Output

Gate Input

"1"

"0"

$V_{OH}$

$V_{OL}$

$V_{IH}$

$V_{IL}$

$\text{NM}_H$

$\text{NM}_L$

Undefined Region

$V_{IL}$

$V_{IH}$
The Regenerative Property

(a) A chain of inverters.

(b) Regenerative gate

(c) Non-regenerative gate
Fan-in and Fan-out

(a) Fan-out $N$

(b) Fan-in $M$
The Ideal Gate

\[ V_{\text{out}} = \begin{cases} V_{\text{in}} & \text{for } V_{\text{in}} < g = -\infty \\ 0 & \text{for } V_{\text{in}} \geq g = -\infty \end{cases} \]

- \( R_i = \infty \)
- \( R_o = 0 \)
VTC of Real Inverter

![VTC Graph](attachment:VTC.png)
Delay Definitions

\[ V_{in} \]

\[ V_{out} \]

- \( t_{pHL} \)
- \( t_{pLH} \)
- \( t_f \)
- \( t_r \)

50% 50%
10% 90%
Ring Oscillator

![Ring Oscillator Diagram]

\[ T = 2 \times t_p \times N \]
Power Dissipation

\[
P_{\text{peak}} = i_{\text{peak}} V_{\text{supply}} = \max(p(t)))
\]

\[
P_{\text{av}} = \frac{1}{T} \int_{0}^{T} p(t) \, dt = \frac{V_{\text{supply}}}{T} \int_{0}^{T} i_{\text{supply}}(t) \, dt
\]

Power-Delay Product

\[
PDP = t_p \times P_{\text{av}}
\]

= Energy dissipated per operation
CMOS INVERTER
The CMOS Inverter: A First Glance
CMOS Inverters

PMOS

Polysilicon

NMOS

In

Out

Metal1

V_DD

1.2 \mu m = 2 \lambda

GND

Inverter

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Switch Model of CMOS Transistor

- $|V_{GS}| < |V_T|$ (low resistance, high conductance)
- $|V_{GS}| > |V_T|$ (high resistance, low conductance)
CMOS Inverter: Steady State Response

\[ V_{out} = \begin{cases} V_{DD} & \text{if } V_{in} = V_{DD} \\ 0 & \text{if } V_{in} = 0 \end{cases} \]

\[ V_{OH} = V_{DD} \]
\[ V_{OL} = 0 \]

\[ V_M = f(R_{on}, R_{onp}) \]
CMOS Inverter: Transient Response

\[ V_{out} = V_{DD} \]

\[ V_{in} = V_{DD} \]

\[ R_{on} \]

\[ C_L \]

\[ t_{pHL} = f(R_{on} \cdot C_L) = 0.69 \cdot R_{on} \cdot C_L \]

\[ \ln(0.5) \]

\[ V_{out} \]

\[ V_{DD} \]

\[ 0.5 \]

\[ 0.36 \]

\[ t \]

\[ R_{on} \cdot C_L \]
CMOS Properties

- Full rail-to-rail swing
- Symmetrical VTC
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation
- Direct path current during switching
Voltage Transfer Characteristic
PMOS Load Lines

\[ V_{in} = V_{DD} - V_{GSp} \]
\[ I_{Dn} = -I_{Dp} \]
\[ V_{out} = V_{DD} - V_{DSP} \]
CMOS Inverter Load Characteristics
CMOS Inverter VTC

V_{out} \uparrow

1 2 3 4 5

NMOS off
PMOS lin

NMOS sat
PMOS lin

NMOS sat
PMOS sat

NMOS lin
PMOS sat

NMOS lin
PMOS off

V_{in}
Simulated VTC

![VTC Graph](image)
Gate Switching Threshold

\[ V_M = \frac{r(V_{DD} - |V_{TP}|) + V_{TN}}{1 + r} \quad \text{with} \quad r = \sqrt{\frac{k_P}{k_n}} \]
MOS Transistor Small Signal Model

\[
g_m V_{gs} \quad r_o
\]

<table>
<thead>
<tr>
<th></th>
<th>( g_m )</th>
<th>( r_o )</th>
</tr>
</thead>
<tbody>
<tr>
<td>linear</td>
<td>( kV_{DS} )</td>
<td>([k(V_{GS}-V_T-V_{DS})]^{-1})</td>
</tr>
<tr>
<td>saturation</td>
<td>( k(V_{GS}-V_T) )</td>
<td>(1/\lambda I_D)</td>
</tr>
</tbody>
</table>

Digital Integrated Circuits

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Determining $V_{IH}$ and $V_{IL}$

At $V_{IH}$ ($V_{IL}$):

$$\frac{\partial V_{out}}{\partial V_{in}} = -1$$

small-signal model of inverter

$$g = \frac{v_{out}}{v_{in}} = -(g_{mn} + g_{mp}) \times (r_{on} \parallel r_{op}) = -1$$
Propagation Delay
CMOS Inverter: Transient Response

\[ V_{\text{DD}} \]

\[ V_{\text{in}} = V_{\text{DD}} \]

\[ R_{\text{on}} \]

\[ C_{L} \]

\[ V_{\text{out}} \]

\[ t_{\text{pHL}} = f(R_{\text{on}} \cdot C_{L}) \]

\[ = 0.69 R_{\text{on}} C_{L} \]
CMOS Inverter Propagation Delay

\[ t_{pHL} = \frac{C_L \cdot V_{swing}}{2 \cdot I_{av}} \]

\[ \sim \frac{C_L}{k_n \cdot V_{DD}} \]
Computing the Capacitances

Simplified Model

Fanout

Interconnect

Inverter

CMOS Inverters
The Miller Effect

“A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value.”
Computing the Capacitances

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{gd1}$</td>
<td>$2 \text{ CGD0 } W_n$</td>
</tr>
<tr>
<td>$C_{gd2}$</td>
<td>$2 \text{ CGD0 } W_p$</td>
</tr>
<tr>
<td>$C_{db1}$</td>
<td>$K_{eqn} (AD_n CJ + PD_n CJSW)$</td>
</tr>
<tr>
<td>$C_{db2}$</td>
<td>$K_{eqp} (AD_p CJ + PD_p CJSW)$</td>
</tr>
<tr>
<td>$C_{g3}$</td>
<td>$C_{ox} W_n L_n$</td>
</tr>
<tr>
<td>$C_{g4}$</td>
<td>$C_{ox} W_p L_p$</td>
</tr>
<tr>
<td>$C_w$</td>
<td>From Extraction</td>
</tr>
<tr>
<td>$C_L$</td>
<td>$\sum$</td>
</tr>
</tbody>
</table>
Impact of Rise Time on Delay

\[ t_{pHL} = \sqrt{t_{pHL,\text{step}}^2 + \left(\frac{t_r}{2}\right)^2} \]
Delay as a function of $V_{DD}$
Where Does Power Go in CMOS?

• Dynamic Power Consumption
  Charging and Discharging Capacitors

• Short Circuit Currents
  Short Circuit Path between Supply Rails during Switching

• Leakage
  Leaking diodes and transistors
Dynamic Power Dissipation

Energy/transition = $C_L \times V_{dd}^2$

Power = Energy/transition * $f = C_L \times V_{dd}^2 \times f$

- Not a function of transistor sizes!
- Need to reduce $C_L$, $V_{dd}$, and $f$ to reduce power.
Impact of Technology Scaling
## Technology Evolution

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length ((\mu)m)</td>
<td>0.4</td>
<td>0.3</td>
<td>0.25</td>
<td>0.18</td>
<td>0.13</td>
<td>0.1</td>
</tr>
<tr>
<td>Gate oxide (nm)</td>
<td>12</td>
<td>7</td>
<td>6</td>
<td>4.5</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>(V_{DD}) (V)</td>
<td>3.3</td>
<td>2.2</td>
<td>2.2</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>(V_T) (V)</td>
<td>0.7</td>
<td>0.7</td>
<td>0.7</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
</tr>
<tr>
<td>NMOS (I_{Dsat}) (mA/(\mu)m) (@ (V_{GS} = V_{DD}))</td>
<td>0.35</td>
<td>0.27</td>
<td>0.31</td>
<td>0.21</td>
<td>0.29</td>
<td>0.33</td>
</tr>
<tr>
<td>PMOS (I_{Dsat}) (mA/(\mu)m) (@ (V_{GS} = V_{DD}))</td>
<td>0.16</td>
<td>0.11</td>
<td>0.14</td>
<td>0.09</td>
<td>0.13</td>
<td>0.16</td>
</tr>
</tbody>
</table>
Technology Scaling (1)

Minimum Feature Size
Technology Scaling (2)

Number of components per chip
Propagation Delay Scaling

![Graph showing propagation delay scaling with channel length and gate delay](image)

- Gate Delay: $t_p$ (ps/week)
- Channel Length: $L_{eq} (\mu m)$
- Voltage levels: 5 V, 3.5 V, 3.3 V, 2.5 V
Technology Scaling Models

• Full Scaling (Constant Electrical Field)
  ideal model — dimensions and voltage scale together by the same factor $S$

• Fixed Voltage Scaling
  most common model until recently —
  only dimensions scale, voltages remain constant

• General Scaling
  most realistic for today’s situation —
  voltages and dimensions scale with different factors
# Scaling Relationships for Long Channel Devices

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Relation</th>
<th>Full Scaling</th>
<th>General Scaling</th>
<th>Fixed Voltage Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W, L, t_{ox}$</td>
<td>$1/S$</td>
<td>$1/S$</td>
<td>$1/S$</td>
<td>$1/S$</td>
</tr>
<tr>
<td>$V_{DD}, V_T$</td>
<td>$1/S$</td>
<td>$1/U$</td>
<td>$1$</td>
<td></td>
</tr>
<tr>
<td>$N_{SUB}$</td>
<td>$V/W_{dep}^2$</td>
<td>$S$</td>
<td>$S^2/U$</td>
<td>$S^2$</td>
</tr>
<tr>
<td>Area/Device</td>
<td>$WL$</td>
<td>$1/S^2$</td>
<td>$1/S^2$</td>
<td>$1/S^2$</td>
</tr>
<tr>
<td>$C_{ox}$</td>
<td>$1/t_{ox}$</td>
<td>$S$</td>
<td>$S$</td>
<td>$S$</td>
</tr>
<tr>
<td>$C_L$</td>
<td>$C_{ox}W/L$</td>
<td>$1/S$</td>
<td>$1/S$</td>
<td>$1/S$</td>
</tr>
<tr>
<td>$k_n, k_p$</td>
<td>$C_{ox}W/L$</td>
<td>$S$</td>
<td>$S$</td>
<td>$S$</td>
</tr>
<tr>
<td>$I_{av}$</td>
<td>$k_{n,p} V^2$</td>
<td>$1/S$</td>
<td>$S/U^2$</td>
<td>$S$</td>
</tr>
<tr>
<td>$t_p$ (intrinsic)</td>
<td>$C_L V / I_{av}$</td>
<td>$1/S$</td>
<td>$U/S^2$</td>
<td>$1/S^2$</td>
</tr>
<tr>
<td>$P_{av}$</td>
<td>$C_L V^2 / t_p$</td>
<td>$1/S^2$</td>
<td>$S/U^3$</td>
<td>$S$</td>
</tr>
<tr>
<td>PDP</td>
<td>$C_L V^2$</td>
<td>$1/S^3$</td>
<td>$1/SU^2$</td>
<td>$1/S$</td>
</tr>
</tbody>
</table>

Table 3.1: Scaling Relationships for Long Channel Devices
## Scaling of Short Channel Devices

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Relation</th>
<th>Full Scaling</th>
<th>General Scaling</th>
<th>Fixed Voltage Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{av}$</td>
<td>$C_{ox}WV$</td>
<td>$1/S$</td>
<td>$1/U$</td>
<td>$1$</td>
</tr>
<tr>
<td>$J_{av}$</td>
<td>$I_{av}/\text{Area}$</td>
<td>$S$</td>
<td>$S^2/U$</td>
<td>$S^2$</td>
</tr>
<tr>
<td>$t_p$ (intrinsic)</td>
<td>$C_{LV}/I_{av}$</td>
<td>$1/S$</td>
<td>$1/S$</td>
<td>$1/S$</td>
</tr>
<tr>
<td>$P_{av}$</td>
<td>$C_{LV}^2/t_p$</td>
<td>$1/S^2$</td>
<td>$1/U^2$</td>
<td>$1$</td>
</tr>
</tbody>
</table>
BIPOLAR INVERTERS
Resistor-Transistor Logic

V\text{in} \quad V_{out} \\
R_B \quad Q_1 \quad V_{cc} \\
R_C

V_{CE(sat)} \quad V_{CC} \quad V_{in(eos)} \\
V_{BE(on)} \quad V_{out} \\
Cutoff \quad Saturation \quad Forward-active

VTC of nonsaturating gate
VTC of RTL Inverter

VOH is function of fan-out
Transient Response of RTL Inverter

\[ t_p = 290 \text{ psec} !!!! \]
The ECL Gate at a Glance

Core of gate: The differential pair or “current switch”
Single-ended versus Differential Logic

Single-ended

Differential
Complete ECL Gate

Emitter-follower output driver
The Bias Network

Issues:
- Temperature variations
- Device variations

\[ V_{ref} = V_{B5} - V_{BE(on)} \]

\[ V_{B5} = V_{CC} - \frac{R_1}{R_1 + R_2} (V_{CC} - 2V_D - V_{EE}) \]
Photomicrograph of early ECL Gate (1967)
ECL VTC

\[ V_{out} = V_{CC} - V_{BE(on)} \]

\[ V_{out2} = \pm n \phi_T \]

\[ V_{out1} = V_{CC} - V_{BE(on)} - I_{EE} R_C \]

\[ Q_1 \text{ saturates} \]

\[ V_{ref} \]

\[ V_{in} \]
ECL VTC

\[ V_{\text{swing}} = I_{EE} R_C \]

\[ \frac{I_{C1}}{I_{EE}} = \frac{e^x}{1 + e^x} = \alpha = 0.01 \]

\[ V_{IL, IH} = V_{ref} \pm \phi_T ln \left( \frac{\alpha}{1 - \alpha} \right) \]
Simulated VTC of ECL Gate

![Simulated VTC of ECL Gate](image)
ECL Gate with Single Fan-out
Simulated Collector Currents of Differential Pair

![Graph showing simulated collector currents of a differential pair with normalized collector current on the y-axis and time on the x-axis. The graph includes curves for different currents: 10 mA, 5 mA, 1 mA, and 0.5 mA. The x-axis ranges from 0 to 0.2 nsec. The y-axis ranges from -1 to 1. The curves are labeled as $I_{C1}$ and $I_{C2}$.](image-url)
## Propagation Delay of ECL Gate

<table>
<thead>
<tr>
<th>$t_{pHL}$</th>
<th>$R_B C_L \gg R_C C_C$</th>
<th>$r_B(2.2 C_{inj} + \alpha C_{D1})$</th>
<th>$0.5 C_L R_B \left( \frac{V_{swing}}{V_{CC} - V_{EE}} \right)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_B C_L \ll R_C C_C$</td>
<td>$0.69 \left( \frac{R_C}{\beta_P + 1} \parallel R_B \right) (C_C(\beta_P + 1) + C_L)$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{pLH}$</td>
<td>$r_B(2.2 C_{inj} + \alpha C_{D1})$</td>
<td>$0.69 \left( \frac{R_C}{\beta_P + 1} \parallel R_B \right) (C_C(\beta_P + 1) + C_L)$</td>
<td></td>
</tr>
</tbody>
</table>
Simulated Transient Response of ECL Inverter

![Simulated Transient Response of ECL Inverter Diagram]
Propagation Delay as a Function of Bias Current

![Graph showing the relationship between propagation delay and bias current for an inverter. The x-axis represents the bias current (I_{EE} in mA) and the y-axis represents the propagation delay (t_{p, LH} in psec). The graph shows a decrease in propagation delay as the bias current increases, reaching a minimum around 5 mA, before increasing slightly with further increases in current.]}
ECL Power Dissipation

\[ P_{\text{stat}} = (V_{CC} - V_{EE}) \left( I_{EE} + \frac{I_{bias}}{N} + 2 \frac{V_{OH} + V_{OL}}{2 R_B} - V_{EE} \right) \]

\[ P_{\text{dyn}} = C_T (V_{CC} - V_{EE}) V_{\text{swing}} f \]
### Scaling Model for Bipolar Inverter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Scaling Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_E$</td>
<td>$1/S^2$</td>
</tr>
<tr>
<td>$w_B$</td>
<td>$1/S^{0.8}$</td>
</tr>
<tr>
<td>$V_{\text{supply}}$</td>
<td>1</td>
</tr>
<tr>
<td>$V_{\text{swing}}$</td>
<td>1</td>
</tr>
<tr>
<td>$J$</td>
<td>$S^2$</td>
</tr>
<tr>
<td>$I$</td>
<td>1</td>
</tr>
<tr>
<td>$C_dC_j$</td>
<td>$1/S$</td>
</tr>
<tr>
<td>$t_p$</td>
<td>$1/S$</td>
</tr>
<tr>
<td>$P$</td>
<td>1</td>
</tr>
</tbody>
</table>
Bipolar Scaling

![Graph showing the relationship between gates per chip, lithography level, current, delay, and power consumption.](image)