Low Power Design in CMOS
Why worry about power?
-- Heat Dissipation

microprocessor power dissipation

source: arpa-esto

![Graph showing microprocessor power dissipation vs. die area x clock frequency (cm^2 MHz). The graph includes data points for different manufacturers such as HP, Intel, DEC, DEC 21164, Sun, IBM, and Others.]
Evolution in Power Dissipation

![Graphs showing the evolution of power dissipation over years, with data points for MPU and DSP.]
Why worry about power — Portability

Expected Battery Lifetime increase over next 5 years: 30-40%

Multimedia Terminals
Laptop Computers
Digital Cellular Telephony

Nominal Capacity (Watt-hours / lb)

Year

65 70 75 80 85 90 95

Nickel-Cadmium
Ni-Metal Hydride
Rechargeable Lithium

BATTERY
(40+ lbs)
Where Does Power Go in CMOS?

- **Dynamic Power Consumption**
  - Charging and Discharging Capacitors

- **Short Circuit Currents**
  - Short Circuit Path between Supply Rails during Switching

- **Leakage**
  - Leaking diodes and transistors
Dynamic Power Consumption

\[ \text{Energy/transition} = C_L \times V_{dd}^2 \]

\[ \text{Power} = \text{Energy/transition} \times f = C_L \times V_{dd}^2 \times f \]

- Not a function of transistor sizes!
- Need to reduce \( C_L \), \( V_{dd} \), and \( f \) to reduce power.
Dynamic Power Consumption - Revisited

Power = Energy/transition * transition rate

\[
= C_L * V_{dd}^2 * f_{0\rightarrow 1}
\]

\[
= C_L * V_{dd}^2 * P_{0\rightarrow 1} * f
\]

\[
= C_{EFF} * V_{dd}^2 * f
\]

Power Dissipation is Data Dependent
Function of Switching Activity

\[C_{EFF} = \text{Effective Capacitance} = C_L * P_{0\rightarrow 1}\]
Power Consumption is Data Dependent

Example: Static 2 Input NOR Gate

Assume:
\[ P(A=1) = \frac{1}{2} \]
\[ P(B=1) = \frac{1}{2} \]

Then:
\[ P(\text{Out}=1) = \frac{1}{4} \]
\[ P(0 \rightarrow 1) = P(\text{Out}=0).P(\text{Out}=1) \]
\[ = \frac{3}{4} \times \frac{1}{4} = \frac{3}{16} \]

\[ C_{\text{EFF}} = \frac{3}{16} \times C_L \]
## Transition Probabilities for Basic Gates

<table>
<thead>
<tr>
<th></th>
<th>( P_{0 \to 1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>AND</td>
<td>((1-P_A P_B)P_A P_B)</td>
</tr>
<tr>
<td>OR</td>
<td>((1-P_A)(1-P_B)(1-(1-P_A)(1-P_B)))</td>
</tr>
<tr>
<td>EXOR</td>
<td>((1 - (P_A + P_B - 2P_A P_B))(P_A + P_B - 2P_A P_B))</td>
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Switching Activity for Static CMOS

\[ P_{0 \to 1} = P_0 \cdot P_1 \]
Transition Probability of 2-input NOR Gate

\[ p_1 = (1-p_a) (1-p_b) \]

\[ p_{0 \rightarrow 1} = p_0 \cdot p_1 = (1-(1-p_a) (1-p_b)) (1-p_a) (1-p_b) \]

- \( \alpha_{0 \rightarrow 1} \) is a strong function of signal statistics
Problem: Reconvergent Fanout

\[ P(Z=1) = P(B=1) \cdot P(X=1 \mid B=1) \]

Becomes complex and intractable real fast
How about Dynamic Circuits?

Power is Only Dissipated when Out=0!

\[ C_{\text{EFF}} = P(\text{Out}=0) \cdot C_L \]
4-input NAND Gate

Example: Dynamic 2 Input NOR Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Truth Table of 2 input NOR gate

Assume:
- \( P(A=1) = 1/2 \)
- \( P(B=1) = 1/2 \)

Then:
- \( P(\text{Out}=0) = 3/4 \)

\[ C_{\text{EFF}} = 3/4 \times C_L \]

Switching Activity Is Always Higher in Dynamic Circuits
Transition Probabilities for Dynamic Gates

<table>
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Switching Activity for Precharged Dynamic Gates

$P_{0 \rightarrow 1} = P_0$
Glitching in Static CMOS

also called: dynamic hazards

<table>
<thead>
<tr>
<th>ABC</th>
<th>101</th>
<th>000</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Z</td>
<td></td>
<td></td>
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Unit Delay

Observe: No glitching in dynamic circuits
Example 1: Chain of NOR Gates
Example 2: Adder Circuit
How to Cope with Glitching?

Equalize Lengths of Timing Paths Through Design
Short Circuit Currents

\[ I = \begin{array}{c} \text{Vin} \\text{Vout} \\ \text{Vdd} \end{array} \]

\[ V_{in} (V) \quad 0.15 \quad 0.10 \quad 0.05 \]

\[ V_{out} \]

\[ C_L \]

\[ I_{VDD} (mA) \quad 0.15 \quad 0.10 \quad 0.05 \]

\[ V_{in} (V) \quad 0.0 \quad 1.0 \quad 2.0 \quad 3.0 \quad 4.0 \quad 5.0 \]
Impact of rise/ fall times on short-circuit currents

Large capacitive load

Small capacitive load
Short-circuit energy as a function of slope ratio

The power dissipation due to short circuit currents is minimized by matching the rise/fall times of the input and output signals.

- $V_{DD} = 5$ V
- $V_{DD} = 3.3$ V

$W/L|_P = 7.2\mu m/1.2\mu m$

$W/L|_N = 2.4\mu m/1.2\mu m$
Static Power Consumption

\[ P_{\text{stat}} = P_{(\ln=1)} \cdot V_{dd} \cdot I_{\text{stat}} \]

- Dominates over dynamic consumption
- Not a function of switching frequency
Leakage

Sub-Threshold Current Dominant Factor
Sub-Threshold in MOS

\[ \sqrt{I_D} \]

\[ V_T = 0.2 \quad V_T = 0.6 \quad V_{GS} \]

Lower Bound on Threshold to Prevent Leakage
Power Analysis in SPICE

Equivalent Circuit for Measuring Power in SPICE

\[ C \frac{dP_{av}}{dt} = k i_{DD} \]

or

\[ P_{av} = \frac{k}{C} \int_0^T i_{DD} dt \]
Here it is assumed that $R_p = R_n$
Reducing $V_{dd}$

- Strong function of voltage ($V^2$ dependence).
- Relatively independent of logic function and style.
- Power Delay Product Improves with lowering $V_{DD}$. 

$$P \times t_d = E_t = C_L \times V_{dd}^2$$

\[ \frac{E(V_{dd=2})}{E(V_{dd=5})} = \frac{(C_L) \times (2)^2}{(C_L) \times (5)^2} \]

\[ E(V_{dd=2}) \approx 0.16 \times E(V_{dd=5}) \]
Lower $V_{dd}$ Increases Delay

\[ T_d = \frac{C_L \cdot V_{dd}}{I} \]

\[ I \sim (V_{dd} - V_t)^2 \]

\[
\begin{align*}
T_d(V_{dd}=2) &= \frac{(2) \cdot (5 - 0.7)^2}{(5) \cdot (2 - 0.7)^2} \\
T_d(V_{dd}=5) &= \frac{(2) \cdot (5 - 0.7)^2}{(5) \cdot (2 - 0.7)^2} \\
&\approx 4
\end{align*}
\]

- Relatively independent of logic function and style.
Lowering the Threshold

Reduces the Speed Loss, But Increases Leakage

Interesting Design Approach:

DESIGN FOR $P_{\text{Leakage}} = P_{\text{Dynamic}}$
Transistor Sizing for Power Minimization

- Larger sized devices are useful only when interconnect dominated.
- Minimum sized devices are usually optimal for low-power.
Transistor Sizing for Fixed Throughput

\[ C_g = \frac{W}{L} C_{\text{MIN}} \]

\[ C_P = C_{\text{wiring}} + C_{\text{DF}} \]

**HIGH PERFORMANCE**

\[ W/L \gg C_P / (K C_{\text{MIN}}) \]

**LOW POWER**

\[ W/L = 2 \frac{C_P}{(K C_{\text{MIN}})} \]

(if \( C_P \geq K C_{\text{MIN}} \))

ELSE \( W/L = 1 \)

\[ \alpha = C_P / (K C_{\text{MIN}}) \]

\[ C_{\text{MIN}} = \text{Minimum sized gate (W/L=1)} \]

\[ W/L \text{ after sizing} \]

**Diagram:**

- \( \alpha = 0 \)
- \( \alpha = 0.5 \)
- \( \alpha = 1 \)
- \( \alpha = 1.5 \)
- \( \alpha = 2 \)

**Curves:**

- **adder**

**Axes:**

- **NORMALIZED ENERGY**
- **W/L**

Reducing Effective Capacitance

Global bus architecture

Local bus architecture

Shared Resources incur Switching Overhead
Summary

• Power Dissipation is becoming Prime Design Constraint

• Low Power Design requires Optimization at all Levels

• Sources of Power Dissipation are well characterized

• Low Power Design requires operation at lowest possible voltage and clock speed