SEQUENTIAL LOGIC
Sequential Logic

2 storage mechanisms
- positive feedback
- charge-based
Positive Feedback: Bi-Stability
Meta-Stability

Gain should be larger than 1 in the transition region
SR-Flip Flop

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>( \overline{Q} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q</td>
<td>Q</td>
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<td>0</td>
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<td>0</td>
<td>0</td>
<td>1</td>
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</table>
JK-Flip Flop

(a)

(b)

(c)

<table>
<thead>
<tr>
<th>J_n</th>
<th>K_n</th>
<th>Q_{n+1}</th>
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<td>0</td>
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<td>Q_n</td>
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<td>0</td>
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<tr>
<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>\bar{Q}_n</td>
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Digital Integrated Circuits
Sequential Logic
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Other Flip-Flops

Toggle Flip-Flop

Delay Flip-Flop
Race Problem

Signal can race around during $\phi = 1$
Master-Slave Flip-Flop
Propagation Delay Based Edge-Triggered

\[
\begin{align*}
\text{In} & \quad \text{N1} & \quad X & \quad \text{N2} & \quad \text{Out} \\
\phi & \quad \text{In} & \quad \text{Out} \\
\end{align*}
\]

\[t_{PLH} = \text{Mono-Stable Multi-Vibrator}\]
Edge Triggered Flip-Flop
Flip-Flop: Timing Definitions

In

Out

\[ \phi \]

\[ t \]

\[ t_{\text{setup}} \quad t_{\text{hold}} \]

\[ \text{DATA STABLE} \]

\[ t_{\text{pFF}} \]

\[ \text{DATA STABLE} \]
Maximum Clock Frequency

\[ t_{p,FF} + t_{p,comb} + t_{setup} < T \]
CMOS Clocked SR-FlipFlop
Flip-Flop: Transistor Sizing
6 Transistor CMOS SR-Flip Flop
Charge-Based Storage

(a) Schematic diagram

(b) Non-overlapping clocks

Pseudo-static Latch
Master-Slave Flip-Flop

Overlapping Clocks Can Cause
- Race Conditions
- Undefined Signals
2 phase non-overlapping clocks
2-phase dynamic flip-flop
Flip-flop insensitive to clock overlap

C²MOS LATCH
C\textsuperscript{2}MOS avoids Race Conditions

(a) (1-1) overlap

(b) (0-0) overlap
Pipelining

Non-pipelined version

Pipelined version

<table>
<thead>
<tr>
<th>Clock Period</th>
<th>Adder</th>
<th>Absolute Value</th>
<th>Logarithm</th>
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<tbody>
<tr>
<td>1</td>
<td>$a_1 + b_1$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>$a_2 + b_2$</td>
<td>$</td>
<td>a_1 + b_1</td>
</tr>
<tr>
<td>3</td>
<td>$a_3 + b_3$</td>
<td>$</td>
<td>a_2 + b_2</td>
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<tr>
<td>4</td>
<td>$a_4 + b_4$</td>
<td>$a_3 + b_3$</td>
<td>$\log(</td>
</tr>
<tr>
<td>5</td>
<td>$a_5 + b_5$</td>
<td>$a_4 + b_4$</td>
<td>$\log(</td>
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Pipelined Logic using $C^2$MOS

NORA CMOS

What are the constraints on $F$ and $G$?
Example

Number of a static inversions should be even
NORA CMOS Modules
Doubled $C^2$MOS Latches

Doubled n-$C^2$MOS latch

Doubled n-$C^2$MOS latch
TSPC - True Single Phase Clock Logic

Including logic into the latch

Inserting logic between latches
Master-Slave Flip-flops

(a) Positive edge-triggered $D$ flip-flop
(b) Negative edge-triggered $D$ flip-flop
(c) Positive edge-triggered $D$ flip-flop using split-output latches
Schmitt Trigger

• VTC with hysteresis
• Restores signal slopes
Noise Suppression using Schmitt Trigger
CMOS Schmitt Trigger

Moves switching threshold of first inverter
Schmitt Trigger
Simulated VTC
CMOS Schmitt Trigger (2)
Multivibrator Circuits

- Bistable Multivibrator
  - flip-flop, Schmitt Trigger

- Monostable Multivibrator
  - one-shot

- Astable Multivibrator
  - oscillator
Transition-Triggered Monostable

In

DELAY

Out

$td$

$td$
Monostable Trigger (RC-based)

(a) Trigger circuit.

(b) Waveforms.
Astable Multivibrators (Oscillators)

Ring Oscillator

simulated response of 5-stage oscillator
Voltage Controller Oscillator (VCO)

Current starved inverter

Schmitt Trigger restores signal slopes

propagation delay as a function of control voltage
Relaxation Oscillator

\[ T = 2 \log_3 RC \]