Lecture 6:
CMOS Proximity Wireless Communications for 3D Integration (1)

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Trend of Chip Performance and Pin Bandwidth

Chip Performance

- 4004
- 8086
- 286
- Intel386
- Intel486
- Pentium
- Pentium4

Year
- 70
- 80
- 90
- 00
- 10

MIPS [instruction/s]
- 0.01
- 0.1
- 1
- 10
- 100
- 1000
- 10000
- 100000
- 1000000

Pin Bandwidth

- ATA (HDD)
- Ethernet
- ISA
- PCI
- PCI-EX
- Serial ATA
- Fast Ethernet

Data Rate [MB/s]
- 1
- 10
- 100
- 1000
- 10000
- 100000
- 1000000

Year
- 60
- 90
- 00
- 10

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Courtesy: Intel, Fujitsu Lab
The Gap Is Caused by Topological Difference

**Moore’s Law**

<table>
<thead>
<tr>
<th>TRANSISTOR</th>
<th>Scaling</th>
<th>Per year</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate length</td>
<td>$[x]$</td>
<td>0.87</td>
</tr>
<tr>
<td>Voltage</td>
<td>$[V]$</td>
<td>0.87</td>
</tr>
<tr>
<td>Capacitance</td>
<td>$[C] \sim [x^2/x]$</td>
<td>0.87</td>
</tr>
<tr>
<td>Current</td>
<td>$[i] \sim [v^2/x]$</td>
<td>0.87</td>
</tr>
<tr>
<td>Speed</td>
<td>$[i/cv]$</td>
<td>1.15</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>WIRE</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire pitch</td>
<td>$[x]$</td>
<td>0.87</td>
</tr>
<tr>
<td>Chip size</td>
<td>$[s]$</td>
<td>1.06</td>
</tr>
<tr>
<td>Tracks</td>
<td>$[t] \sim [s/x]$</td>
<td>1.22</td>
</tr>
<tr>
<td>Grids</td>
<td>$[g] \sim [t^2]$</td>
<td>1.49</td>
</tr>
</tbody>
</table>

**Rent’s rule:**

Bandwidth demand from a module with capacity $C$ (grids*speed) grows as $C^{0.7}$.

Required pin bandwidth: x1.45/year

**Chip performance**

1.15 (Speed) x 1.49 (Grids) = x1.71/year

**Pin bandwidth**

1.15 (Speed) x 1.11 (Pin #) = x1.28/year

Area

Periphery

**Moore’s Law**

- Scaling: 1.28/year
  - Chip performance: 1.71/year
  - Pin bandwidth: 1.45/year

**Area**

**Periphery**

**Scaling: 1.28/year**

**Data Rate**
Challenges in Wireline Link

Power/Area-wall

Speed-wall

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Leakage and IO Power Rapidly Increasing

150nm and 65nm Single-chip Supercomputer at Max Performance

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I/O Power Recently Increasing

\[ fC V^2 \propto \frac{1}{\kappa^{1.3}} \]
I/O Power Details

<table>
<thead>
<tr>
<th>Power [mW]</th>
<th>90nm, 10Gb/s</th>
<th>180nm, 2.5Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>150</td>
<td>25mW, 10%</td>
</tr>
<tr>
<td>200</td>
<td>200</td>
<td>70mW, 30%</td>
</tr>
<tr>
<td>100</td>
<td>25mW, 10%</td>
<td>25mW, 10%</td>
</tr>
<tr>
<td>0</td>
<td>25mW, 10%</td>
<td>25mW, 10%</td>
</tr>
<tr>
<td>150</td>
<td>30mW, 12%</td>
<td>25mW, 21%</td>
</tr>
<tr>
<td>250</td>
<td>20mW, 17%</td>
<td>20mW, 17%</td>
</tr>
<tr>
<td>90nm, 10Gb/s</td>
<td></td>
<td>5mW, 4%</td>
</tr>
<tr>
<td>20mW, 17%</td>
<td>25mW, 21%</td>
<td>10mW, 8%</td>
</tr>
<tr>
<td>25mW, 21%</td>
<td>25mW, 10%</td>
<td>25mW, 10%</td>
</tr>
<tr>
<td>5mW, 4%</td>
<td>25mW, 10%</td>
<td>25mW, 10%</td>
</tr>
<tr>
<td>10mW, 8%</td>
<td>15mW, 6%</td>
<td>15mW, 6%</td>
</tr>
<tr>
<td>Other</td>
<td>245mW</td>
<td>120mW</td>
</tr>
</tbody>
</table>

Power in red is increasing
+5% Speed Requires +20% Power in Clock

Normalized speed
(by changing the number & size of repeaters)

Normalized power

exponential

Ref. [11]
SoC Improves I/O Performance

- 70% power reduction by DRAM embedding technology

Embedded DRAM

- DRAM
- Logic & memory
- DRAM - logic interface
- MPEG4 codec
- Multiplexer
- Speech codec
- 16Mbit DRAM

Separate chips

- 891mW
- 240mW

Power

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From SoC to SiP

System-on-a-Board

System-in-a-Package (SiP)

Lower Cost, QTAT

Low power, High speed

System-on-a-Chip (SoC)

Number of design starts is declining from 1997.

Source: EE Times

Source: Intel
Chip Stacking and Wire Bonding in SiP

Courtesy: Toshiba
From Periphery to Area

- **Bonding (Conv.)**
  (+) low cost, practical
  (-) peripheral contact:
    small # of connections
    (~100)
  long distance (~10mm)

- **Through Si Via (Future)**
  (+) area contact:
    large # of connections (~10000)
    short distance (~0.1mm)
  (-) expensive process / reliability issue
  (-) low yield due to Known Good Die issue: difficult to test in fine pitch
  (-) scaling limit due to mechanical contacts (~10µm pitch)
From Mechanical to Electrical

- **TSV**
  - (-) process
  - (-) KGD
  - (-) scaling limit

- **Wireless Interface**
  - (+) no addition in process, no reliability issue
  - (+) KGD solvable: easy to attach and remove
  - (+) high density channels (below 10 μm pitch)
  - (+) 3D scaling scenario (thinning a chip)
  - (+) channels through active devices
  - (+) low power: no ESD protection required

Proposal
wireless transceiver arrays
Communication Bottleneck Resolved in SiP

Electrical Area Interface for 3D Integration

Data Rate

Chip performance: 1.71/year
Pin bandwidth: 1.45/year
Scaling: 1.28/year

Year

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# Area Interface for 3D Integration

<table>
<thead>
<tr>
<th></th>
<th>Wired</th>
<th>Wireless</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>2 Chips</strong></td>
<td><img src="image" alt="Micro-Bump" /> [1]</td>
<td><img src="image" alt="Capacitive Coupling" /> [3]</td>
</tr>
<tr>
<td>Face-to-Face</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Over 3 Chips</strong></td>
<td><img src="image" alt="Through-Si Via" /> [2]</td>
<td><img src="image" alt="Inductive Coupling" /> [4]</td>
</tr>
<tr>
<td>Face up/dn</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[1] ISSCC’04, Sony  
[2] ISSCC’01, MIT  

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Capacitive-Coupling Link

- **Chip to Interposer**

  - DC connection (Solder bump)
  - AC connections
  - DC connection (Solder bump)

  - Trench
  - Interconnection layer
  - Substrate

- **Chip to Chip**

  - Face-down chips
  - 30um pitch mini-pads (Top metal layer)

  - Base chip

[7] CICC’05, Univ. Bologna

© T. Kuroda (16/48)
Inductive-Coupling Link

Multi-layer Wires

Digital CMOS Circuits

ISSCC 2004 (1Gb/s)
ISSCC 2005 (200Gb/s)
ISSCC 2006 (1Tb/s)

VLSI 2005
VLSI 2006

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Inductive vs. Capacitive: Loss by Body

Loss = \exp(-T\sqrt{\omega/2\rho}) \ [12]

- **Capacitive**: only for 2 chips, placed face-to-face
- **Inductive**: for 2 chips (face-to-face) and \( \geq 3 \) chips (face up/down)

© T. Kuroda (18/48)
Inductive vs. Capacitive: Package Flexibility

**Inductive Coupling**
- Inductive: compatible with conventional wire/area bonding

**Capacitive Coupling**
- Capacitive: need new technology for power delivery
Inductive vs. Capacitive: Scalability

- Transmission power can be secured even at low $V_{DD}$'s.
- Coupling coefficient is enlarged by increasing # of metal layers.

Supply Voltage $V_{DD}$ [V]

<table>
<thead>
<tr>
<th>Normalized Transmission Power</th>
<th>Inductive</th>
<th>Capacitive</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2</td>
<td>1</td>
<td>0.8</td>
</tr>
<tr>
<td>1.0</td>
<td>0.9</td>
<td>0.7</td>
</tr>
<tr>
<td>0.8</td>
<td>0.8</td>
<td>0.6</td>
</tr>
<tr>
<td>0.6</td>
<td>0.6</td>
<td>0.4</td>
</tr>
<tr>
<td>0.4</td>
<td>0.4</td>
<td>0.2</td>
</tr>
</tbody>
</table>

Normalized $S_{21}$

<table>
<thead>
<tr>
<th>Inductive</th>
<th>Capacitive</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>10</td>
</tr>
<tr>
<td>13</td>
<td>12</td>
</tr>
<tr>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

Number of Metal Layers

<table>
<thead>
<tr>
<th>Normalized $S_{21}$</th>
<th>Inductive</th>
<th>Capacitive</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 µm</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>15 µm</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>20 µm</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>25 µm</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>30 µm</td>
<td>30</td>
<td>30</td>
</tr>
</tbody>
</table>
Channel Design

Modeling

\[
\frac{V_R}{V_T} = \frac{1}{1 + j\omega C_R R_T} \times j\omega k \sqrt{L_T L_R} \times \frac{1}{R_{out}(1 - \omega^2 L_T C_T) + R_T + j\omega (C_T R_T R_{out} + L_T)}
\]

Design knowledge

Optimization

NRZ vs. BPM

- **NRZ Signal**
- **Crosstalk**
- **Rx Dead Zone**

**Graph:**
- BER vs. Pulse Energy
  - NRZ
  - BPM
  - BPM x1/3
  - BPM x1/6

**Diagram:**
- Schematic of Tx and Rx with labels:
  - Txdata
  - Txclk
  - Rxdata
  - I_T
  - V_R

**Time [ns]:**
- 0
- 1.8
- 0
- 1.8
- Txclk

**VR [mV]:**
- 0
- -50
- 0
- 50

**Txdata, Txclk [V]:**
- 0
- 1
- 1
- 0
- 0

**Pulse Energy [pJ/b]:**
- 10^-12
- 10^-9
- 10^-6
- 10^-3

**BER:**
- 10^-15

© T. Kuroda (22/48)
Transceiver Circuit for Data

[14] ISSCC’06, Keio Univ.
Transceiver Circuit for Clock


© T. Kuroda (24/48)
Clock and Data Link

- Both clock and data are linked by inductive coupling

Clock Link

Data Link (one clock latency)

[14] ISSCC’06, Keio Univ.
## LAN Wire vs. Wireless

<table>
<thead>
<tr>
<th>Wired LAN (Ethernet)</th>
<th>Wireless LAN (WiFi)</th>
</tr>
</thead>
<tbody>
<tr>
<td>802.3u (100BASE-T)</td>
<td>802.11b</td>
</tr>
<tr>
<td>twisted pair</td>
<td>2.4GHz</td>
</tr>
<tr>
<td>&lt;100m</td>
<td>&lt;100m</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Data rate</td>
<td></td>
</tr>
<tr>
<td>High speed (100Mbps)</td>
<td>Low speed (11Mbps)</td>
</tr>
<tr>
<td>Reliability</td>
<td></td>
</tr>
<tr>
<td>High (BER&lt;10^{-14})</td>
<td>Low (BER~10^{-4})</td>
</tr>
<tr>
<td>Cost</td>
<td></td>
</tr>
<tr>
<td>Inexpensive (~$15)</td>
<td>Expensive (~$100)</td>
</tr>
<tr>
<td>Power</td>
<td></td>
</tr>
<tr>
<td>Low (~100mA)</td>
<td>High (~400mA)</td>
</tr>
<tr>
<td>Size</td>
<td></td>
</tr>
<tr>
<td>Small</td>
<td>Large (w/ antenna)</td>
</tr>
<tr>
<td>Connection</td>
<td></td>
</tr>
<tr>
<td>Easy (plug and play)</td>
<td>Complex (authentication)</td>
</tr>
<tr>
<td>Usability</td>
<td></td>
</tr>
<tr>
<td>Messy/Difficult (ie.wall)</td>
<td>Neat, Simple, Easy</td>
</tr>
<tr>
<td>Mobility</td>
<td></td>
</tr>
<tr>
<td>Low/Immobile</td>
<td>Movable</td>
</tr>
</tbody>
</table>

Multiple access in free space: cell, TDMA, FDMA, CDMA

- path loss
- multi-path fading

© T. Kuroda (26/48)
### Inter-Chip 3D Link: Wire vs. Wireless

<table>
<thead>
<tr>
<th>Wired Inter-Chip Link</th>
<th>Wireless Inter-Chip Link</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micro-bump (2 chips)</td>
<td>Capacitive coupling (2 chips)</td>
</tr>
<tr>
<td>TSV (&gt;3 chips)</td>
<td>Inductive coupling (&gt;3 chips)</td>
</tr>
<tr>
<td>&lt;100µm</td>
<td>&lt;100µm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Data rate</th>
<th>High speed</th>
<th>Low speed ?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reliability</td>
<td>High-reliable</td>
<td>Low-reliable ?</td>
</tr>
<tr>
<td>Cost</td>
<td>Inexpensive</td>
<td>Expensive ?</td>
</tr>
<tr>
<td>Power</td>
<td>Low</td>
<td>High ?</td>
</tr>
<tr>
<td>Size</td>
<td>Small</td>
<td>Large (w/ Antenna) ?</td>
</tr>
<tr>
<td>Connection</td>
<td>Easy (plug on play)</td>
<td>Complex ?</td>
</tr>
<tr>
<td>Usability</td>
<td>Messy/Difficult (ie. wall)</td>
<td>Neat, Simple, Easy ?</td>
</tr>
<tr>
<td>Mobility</td>
<td>Low/Immobile</td>
<td>Movable ?</td>
</tr>
</tbody>
</table>

100m : 1000 wave length  
100µm : 0.001 wave length (proximity)

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World Fastest (1Tb/s) Data Rate

Power/Area Wall

- Hitachi (1024ch, 12W)
- NEC (4ch, 5W)
- NEC (21ch, 5W)
- NEC (20ch, 8W)
- TI (20ch 6W)
- Rambus FlexIO (48ch, 6W)
- Sony (1300ch), TeraChip (16ch, 15W)
- NTT (32ch, 15W)
- Hotrail (32ch)
- Toshiba (4ch, 4W)
- Rambus (26ch)
- NEC (4ch, 5W)
- NEC (1ch)
- Stanford (1ch)

Speed Wall

- Keio (1Gb/s/ch, 1024ch, 3W)
- Keio (1ch, 46mW)

Year

- ’96
- ’98
- ’00
- ’02
- ’04
- ’06

[14] ISSCC’06, Keio Univ.

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Maximum Data Rate per Channel

\[ f_{SR} = 1/2\pi\sqrt{LC} \]

\[ f_{SR}/3 \]

Communication Distance, \( X \) [\( \mu \text{m} \)]

<table>
<thead>
<tr>
<th>Communication Distance, ( X ) [( \mu \text{m} )]</th>
<th>Maximum Data Rate [Gb/s]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1000</td>
</tr>
<tr>
<td>20</td>
<td>100</td>
</tr>
<tr>
<td>40</td>
<td>10</td>
</tr>
<tr>
<td>60</td>
<td>1</td>
</tr>
<tr>
<td>80</td>
<td>0.1</td>
</tr>
<tr>
<td>100</td>
<td>0.01</td>
</tr>
<tr>
<td>120</td>
<td>0.001</td>
</tr>
</tbody>
</table>

[17] Symp. on VLSI Circuits’06, Keio Univ.
Communication Distance vs. Inductor Size

Receiver
Lower Limits
Comparator

LNA + Comparator (40dB)

LNA noise floor
… difficult to eavesdrop
Bus Probing for Debugging

[20.3] “An Attachable Wireless Chip-Access Interface for Arbitrary Data Rate Using Pulse-Based Inductive-Coupling through LSI Package”

© T. Kuroda (31/48)
World Lowest Energy (0.14pJ/b)

300Gb/s, 6W (20pJ/b), 3.8mm²
1Tb/s, 0.14W (0.14pJ/b), 1mm²

[20.2] “A 0.14pJ/b Inductive-Coupling Inter-Chip Data Transceiver with Digitally-Controlled Precise Pulse Shaping”

© T. Kuroda (32/48)
World Smallest (1mm²/Tb/s)

- L-coupling
  - 30µm pitch (incl. transceiver circuits)
  - Thinner packaging (no solder bump)

- Micro-bump
  - 60µm pitch

- TSV
  - 50µm pitch (excl. transceiver circuits)
  - Need additional area for circuits

[14] ISSCC’06, Keio Univ.
Channel Pitch vs. Crosstalk

![Graph showing the relationship between channel pitch and normalized crosstalk. The graph illustrates the interference-to-signal ratio (ISR) in dB as a function of channel pitch Y [μm]. The x-axis represents channel pitch Y [μm] ranging from 120 to 1200, while the y-axis represents normalized crosstalk ranging from 1 to 10^-4. The ISR is plotted against Y/D, with BER=10^-12 indicated. The graph also includes an inset showing an inductor array with dimensions X and Y, and the notation X=D is used to denote the relationship between these variables.]

[19] CICC’04, Keio Univ.

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Narrower Pitch by Time Interleaving

Received Voltage [mV]

Ch Array

w/o Time Interleaving

2-phase Time Interleaving

4-phase Time Interleaving

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As Reliable As Wireline  (BER<10^{-13})

- Easy to synchronize

1GHz Clock

Data Tx

Data Rx

Error Counter

Timing Margin=150ps

[14] ISSCC’06, Keio Univ.

© T. Kuroda (36/48)
Interference Immunity

- Interference from environment: negligibly small for receiver diminishing by scaling
- Interference to circuits: negligibly small for digital

**Graphs:**
- Magnetic Field Intensity, $B_{EMI}$ [mG]
- Noise Voltage, $V_N$ [mV]
- Frequency [Hz]
- Position, $Y$ [$\mu$m]

**Diagram:**
- Signal Line
- TX
- M1
- M2
- $D=60\mu$m
- $I_T = 5mA$
- 125ps
Misalignment Tolerance

- 3µm alignment error can be compensated by 5% power increase.

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Cost Down

- Circuit solution in standard CMOS:
  no need for new process development
  no additional cost in manufacturing

- Reduce chip size:
  no peripheral circuits needed
  no ESD protection needed
AC Coupling

- No need for level shifters under different $V_{DD}$’s
- No need for additional $V_{DD}$’s nor thick gate oxide transistors
- $V_{DD}$’s can change: in burn-in, dynamic voltage scaling

Chip1, $V_{DD}=1V$

Chip2, $V_{DD}=2V$

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Detachable

- At-speed test possible if same transceiver are arranged in test head:
  - solve KGD problem
  - improve yield
  - remove built-in test circuit
- Wafer entirely test possible:
  - reduce test time and cost (¥ 3 /min)
- Avoid Pad damage by probe:
  - raise yield
- Replace a high-speed connector:
  - improve reliability
  - reduce cost
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<tr>
<td></td>
<td>&lt;100μm</td>
<td>&lt;100μm</td>
</tr>
<tr>
<td>Data rate</td>
<td>High speed</td>
<td>High speed</td>
</tr>
<tr>
<td>Reliability</td>
<td>High reliable</td>
<td>High reliable</td>
</tr>
<tr>
<td>Cost</td>
<td>Up (new technology)</td>
<td>Down (circuit solution)</td>
</tr>
<tr>
<td>Power</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Size</td>
<td>Small</td>
<td>Small</td>
</tr>
<tr>
<td>Connection</td>
<td>Easy</td>
<td>Easy (clock and data)</td>
</tr>
<tr>
<td>Usability</td>
<td>Good</td>
<td>Better (AC coupling)</td>
</tr>
<tr>
<td>Mobility</td>
<td>One time attachment</td>
<td>Detachable</td>
</tr>
<tr>
<td>Scalability</td>
<td>Mechanical</td>
<td>Electrical ... Scalable</td>
</tr>
</tbody>
</table>

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# Constant Magnetic Field Scaling

<table>
<thead>
<tr>
<th>Factor</th>
<th>Scale</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor Size</td>
<td>$[x]$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Power Supply Voltage</td>
<td>$[V]$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Chip Thickness</td>
<td>$[T]$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Coil Turn Number (Layer #)</td>
<td>$[n]$</td>
<td>$\alpha^{0.8}$</td>
</tr>
<tr>
<td>Current</td>
<td>$[I]$</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Circuit Delay Time</td>
<td>$[\tau]$</td>
<td>$[CVIL]$</td>
</tr>
<tr>
<td>Coil Diameter</td>
<td>$[D]$</td>
<td>$[1/x]$</td>
</tr>
</tbody>
</table>
| Self Inductance                             | $[L]$ | $[n^2D^{1.6}]$           | 1
| Magnetic Coupling Coefficient               | $[k]$ | 1                         |
| Receive Signal                              | $[V_R]$ | $[kn^2D^{1.6}(I/t)]$ | 1
| Crosstalk                                   | $[V_{RS}/V_{RN}]$ | 1                         |
| Data Rate / Channel                         | $[1/\tau]$ | $\alpha$               |
| Channel Number / Area                       | $[1/D^2]$ | $\alpha^2$             |
| Aggregated Data Rate / Area                 | $[1/tD^2]$ | $\alpha^3$             |
| Energy / Bit                                | $[ltV]$ | $1/\alpha^3$            |

## Self Inductance

$L \propto n^2 D^{1.6}$

## Received Signal Voltage

$V_R \propto M \left| \frac{\partial I_T}{\partial t} \right|_{max} = k \sqrt{L_T L_R} \left| \frac{\partial I_T}{\partial t} \right|_{max}$

$= kL \frac{I_D}{t_{pd}} = kn^2 D^{1.6} \frac{I_D}{t_{pd}}$
3D Scaling Scenario

Cost/Performance will be improved by a 3D scaling scenario:

Inductive Coupling Link (Communication)

Field Effect Transistor (Computation)

- Diameter: $1/\alpha$
- Chip Thickness: $1/\alpha$
- Turn: $\alpha^{0.8}$
- Voltage: $1/\alpha$
- Transistor size: $1/\alpha$

Constant Magnetic Field

Constant Electric Field

Cost/Performance will be improved by a 3D scaling scenario:

- Voltage: $1/\alpha$
- Transistor size: $1/\alpha$
- Chip Thickness: $1/\alpha$
- Power Supply Voltage: $[V] 1/\alpha$
- Coil Turn Number (Layer #): $[n] 1/\alpha$
- Current: $[I] 1/\alpha$
- Circuit Delay Time: $[t] 1/\alpha$
- Self Inductance: $[L] 1/[\mu D^{1.6}] 1/\alpha$
- Magnetic Coupling Coefficient: $[k] 1$
- CROSSTALK: $[vRS/vRN] 1$
- Data Rate / Channel: $[1/t] \alpha$
- Channel Number / Area: $[1/D^2] \alpha^2$
- Aggregated Data Rate / Area: $[1/ND^2] \alpha^3$
- Energy / Bit: $[I/\mu V] 1/\alpha^2$

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Trends in Chip Performance and Pin Bandwidth

Chip Performance
X1.70/year

Pin Bandwidth
X1.44/year

Data Rate [MB/s]

Year

MIPS [instruction/s]

Intel 486
Intel 386
Pentium
Pentium 4

Inductive-Coupling Link

Rambus FlexIO

T_{chip} = 150 \mu m

80 \mu m
45 \mu m
25 \mu m

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Which Technology, $\mu$-bump, TSV, Inductive?

- Analog
- Digital

- Tr-link
- Chip-link

- High-end
- Consumer

- Homogeneous
- Heterogeneous

- 2 chips
- >3 chips

- $\mu$-bump
- TSV

- TSV-light
- Inductive

- Inductive
Conclusions

- Inductive and capacitive coupling links are discussed.
- Inductive coupling has advantages over capacitive coupling in terms of coupling strength through body, package flexibility, scalability.
- Inductive coupling can link >2 chips (face up or down), and eliminate ESD protection to lower delay, area, power.
- Inductive coupling bears comparison with TSV/µ-Bump in terms of data rate (1Tb/s), reliability (BER<10^-13), energy dissipation (0.1pJ/b)
- Inductive coupling is applicable to a standard CMOS, and less expensive than TSV/µ-Bump.
- Inductive coupling exhibits high noise immunity and alignment tolerance.
- Inductive coupling provides with AC coupling link and makes interface design easy under multiple/variable V_{DD}'s.
- Inductive coupling may make non-contact testing possible.
- Constant magnetic field scaling scenario by thinning chip thickness is proposed as a new guideline for 3D integration.
To Probe Further


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