Latch Parameters

Delays can be different for rising and falling data transitions

Clock Nonidealities

- **Clock skew**
  - Spatial variation in temporally equivalent clock edges; deterministic + random, $t_{SK}$
- **Clock jitter**
  - Temporal variations in consecutive edges of the clock signal; modulation + random noise
  - Cycle-to-cycle (short-term) $t_{JS}$
  - Long term $t_{JL}$
- **Variation of the pulse width**
  - for level sensitive clocking

Flip-Flop Parameters

Delays can be different for rising and falling data transitions

Clock Skew and Jitter

- Both skew and jitter affect the effective cycle time
- Only skew affects the race margin
Clock Skew

<table>
<thead>
<tr>
<th># of registers</th>
<th>Earliest occurrence of Clk edge: Nominal - Tsk/2</th>
<th>Latest occurrence of Clk edge: Nominal + Tsk/2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Clk skew</td>
<td>Insertion delay</td>
<td>Clk delay</td>
</tr>
</tbody>
</table>

Positive and Negative Skew

(a) Positive skew

(b) Negative skew

Constraints on Skew

(a) Race between clock and data

(b) Data should be stable before clock pulse is applied

Longest Logic Path in Edge-Triggered Systems

Clk delay: Tsk, P

Latest point of launching

Earliest arrival of next cycle

Unger and Tan
Trans. on Comp. 10/86

Clock Constraints in Edge-Triggered Systems

If launching edge is late and receiving edge is early, the data will not be too late if:

\[ P - T_{sk} + T_{JS} - T_{SU} \geq T_{clk-QM} + T_{LM} \]

Minimum cycle time is determined by the maximum delays through the logic

\[ P \geq T_{clk-QM} + T_{LM} + T_{SU} + T_{sk} + T_{JS} \]

Double-sided definitions of setup and jitter

Shortest Path

Earliest point of launching

Nominal clock edge

Latest point of launching

Data must not arrive before this time
**Clock Constraints in Edge-Triggered Systems**

If launching edge is early and receiving edge is late:

\[-T_{clk-Qm} + T_{Lm} \geq T_{sk} + T_{H}\]

Minimum logic delay

\[T_{Lm} \geq T_{sk} + T_{H} - T_{clk-Qm}\]

**Flip-Flop – Based Timing**

- **Skew**
- Logic delay
- Flip-flop delay

**Latch timing**

- **φ = 0**
- **φ = 1**

When data arrives to transparent latch

Latch is a ‘soft’ barrier

When data arrives to closed latch

Data has to be ‘re-launched’

**Flip-Flops and Dynamic Logic**

Flip-flops are used only with static logic

**Single-Phase Clock with Latches**

- Unger and Tan Trans. on Comp. 10/86
- **Clk**
- **PW**
- **P**

**Latch-Based Design**

- L1 latch is transparent when \(φ = 0\)
- L2 latch is transparent when \(φ = 1\)
Latch-Based Timing

Can tolerate skew!