CMOS Manufacturing Process

CMOS Process

- Polysilicon
- Al
- SiO$_2$
- $n^+$
- $n^-$
- $p^-$
- $p$-substrate
- n-well
A Modern CMOS Process

Dual-Well Trench-Isolated CMOS Process

Circuit Under Design

This two-inverter circuit (of Figure 3.25 in the text) will be manufactured in a twin-well process.
The Manufacturing Process

For a great tour through the process and its different steps, check
http://www.fullman.com/semiconductors/semiconductors.html

For a complete walk-through of the process (64 steps), check the
Book web-page
http://bwrc.eecs.berkeley.edu/Classes/ICBook
Photo-Lithographic Process

Typical operations in a single photolithographic cycle (from [Fullman]).

Patterning of SiO2

(a) Silicon base material
(b) After oxidation and deposition of negative photoresist
(c) Stepper exposure
(d) After development and etching of resist, chemical or plasma etch of SiO2
(e) After etching
(f) Final result after removal of resist
CMOS Process at a Glance

- Define active areas
- Etch and fill trenches
- Implant well regions
- Deposit and pattern polysilicon layer
- Implant source and drain regions and substrate contacts
- Create contact and via windows
- Deposit and pattern metal layers

CMOS Process Walk-Through

(a) Base material: p+ substrate with p-epi layer

(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

(c) After plasma etch of insulating trenches using the inverse of the active area mask
(d) After trench filling, CMP planarization, and removal of sacrificial nitride

(e) After n-well and $V_{TN}$ adjust implants

(f) After p-well and $V_{TP}$ adjust implants

(g) After polysilicon deposition and etch

(h) After $p^+$ source/drain and $n^+$ source/drain implants. These steps also dope the polysilicon.

(i) After deposition of SiO$_2$ insulator and contact hole etch.
CMOS Process Walk-Through

(j) After deposition and patterning of first Al layer.

(k) After deposition of SiO$_2$ insulator, etching of via’s, deposition and patterning of second layer of Al.

Advanced Metalization
Advanced Metalization

Dual damascene IC process
- Oxide deposition
- Wheel lithography and etchback
- Wire lithography and etchback
- Stencil and wire metal deposition
- Metal chemical mechanical polish

Design Rules

Jan M. Rabaey
3D Perspective

Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  » scalable design rules: lambda parameter
  » absolute dimensions (micron rules)
CMOS Process Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Color</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well (p,n)</td>
<td>Yellow</td>
<td></td>
</tr>
<tr>
<td>Active Area (n+,p+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Select (p+,n+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
<td></td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
<td></td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta</td>
<td></td>
</tr>
<tr>
<td>Contact To Poly</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Contact To Diffusion</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Via</td>
<td>Black</td>
<td></td>
</tr>
</tbody>
</table>

Layers in 0.25 µm CMOS process
Intra-Layer Design Rules

Transistor Layout
Via’s and Contacts

Select Layer
CMOS Inverter Layout

(a) Layout

(b) Cross-Section along A-A'

Layout Editor
Design Rule Checker

Sticks Diagram

- Dimensionless layout entities
- Only topology is important
- Final layout generated by “compaction” program