EE141 – Fall 2005
Lecture 7

Propagation Delay, Power Dissipation

Important!

- Software Lab 3 this week
- Enrollments increased to 86
- Hw-3 due on Thursday 5pm
  • Check it out early (time to ask questions)
Today’s Lecture

- Inverter Performance
- Power Dissipation

Review:

MOS Capacitances: Dynamic Behavior
Capacitive Device Model

\[ C_{GD} = \text{Miller} \]

\[ C_{GS} + C_{GSO} = C_{GCD} + C_{GDO} \]

\[ C_{SB} = C_{\text{diff}} \]

\[ C_{GB} = C_{GCB} \]

Gate-Channel Capacitance

\[ C_{GC} = \text{cut-off} \]

\[ C_{GC} = (2/3)C_{ox}W/L_{eff} \]

\[ C_{GS} = C_{ox}W/L_{eff} \]

\[ C_{GD} = C_{ox}W/L_{eff}/2 \]

\[ C_{DS} = C_{ox}W/L_{eff}/2 \]

\[ C_{DB} = \text{ saturation} \]

\[ C_{GS} = (2/3)C_{ox}W/L_{eff} \]

\[ C_{GD} = \frac{\epsilon_{ox}}{t_{ox}} \]

Off/Linear \[ \rightarrow C_{gate} = C_{ox} \cdot W \cdot L_{eff} \]

Saturation \[ \rightarrow C_{gate} = (2/3) \cdot C_{ox} \cdot W \cdot L_{eff} \]
**Gate Overlap Capacitance**

\[
C_O = C_{ox} \cdot x_d
\]

Off/Lin/Sat \(\rightarrow\) \(C_{GSO} = C_{GDO} = C_O \cdot W\)

**Diffusion Capacitance**

\[
C_{diff} = C_{bottom} + C_{sw} \\
= C_j \cdot AREA + C_{jsw} \cdot PERIMETER
\]

Off/Lin/Sat \(\rightarrow\) \(C_{diff} = C_j \cdot L_S \cdot W + C_{jsw} \cdot (2L_S + W)\)
Capacitive Device Model

- **Gate-Channel Capacitance**
  - \( C_{GC} = C_{ox} \cdot W \cdot L_{eff} \) (Off, Linear)
  - \( C_{GC} = (2/3) \cdot C_{ox} \cdot W \cdot L_{eff} \) (Saturation)

- **Gate Overlap Capacitance**
  - \( C_{GSO} = C_{GDO} = C_{O} \cdot W \) (Always)

- **Junction/Diffusion Capacitance**
  - \( C_{diff} = C_{j} \cdot L_{S} \cdot W + C_{jsw} \cdot (2L_{S} + W) \) (Always)

- Zero-bias \( \rightarrow \) \( C_{diff} > C_{gate} \)
- MOS On \( \rightarrow \) \( C_{diff} \leq C_{gate} \)

Computing the Capacitances

- **Miller effect**
- **Reverse biased junction**
- **Simplified Model**
- **Fanout**

- Off \( \rightarrow \) Sat (M₄)
- Lin (M₃)
- No Miller effect
Computing the Capacitances

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{gd1}$</td>
<td>$\frac{2}{3}CGD0 \ W_n$</td>
</tr>
<tr>
<td>$C_{gd2}$</td>
<td>$\frac{2}{3}CGD0 \ W_p$</td>
</tr>
<tr>
<td>$C_{db1}$</td>
<td>$K_{eqn} \ (AD_n \ CJ + PD_n \ CJSW)$</td>
</tr>
<tr>
<td>$C_{db2}$</td>
<td>$K_{eqn} \ (AD_p \ CJ + PD_p \ CJSW)$</td>
</tr>
<tr>
<td>$C_{g3}$</td>
<td>$C_{ox} \ W_n \ L_n \ (Off \rightarrow Sat^*)$</td>
</tr>
<tr>
<td>$C_{g4}$</td>
<td>$C_{ox} \ W_p \ L_p \ (Lin^*)$</td>
</tr>
<tr>
<td>$C_w$</td>
<td>From Extraction</td>
</tr>
<tr>
<td>$C_L$</td>
<td>$\sum$</td>
</tr>
</tbody>
</table>

* assuming LH transition at $V_{out}$

Reverse biased junction

Miller effect

Propagation Delay
CMOS Inverter Propagation Delay: Approach 1

\[ t_{phL} = \frac{C_L \cdot V_{swing}/2}{I_{avg}} \]

\[ t_{phL} \approx \frac{C_L}{k_n \cdot V_{DD}} \]

CMOS Inverter Propagation Delay: Approach 2

\[ t_{phL} = f(R_{on} \cdot C_L) \]

\[ = 0.69 R_{on} \cdot C_L \]

\[ \ln(0.5) \]
MOS Transistor as a Switch

\[ V_{GS} \geq V_T \]

\[
R_{eq} = \frac{1}{2} \left( R_{mid} + R_0 \right)
\]

\[
R_{eq} = \frac{1}{2} \left( \frac{V_{DD}}{I_{DSAT} \cdot (1 + \lambda \cdot V_{DD})} + \frac{V_{DD} / 2}{I_{DSAT} \cdot (1 + \lambda \cdot V_{DD} / 2)} \right)
\]

\[
R_{eq} \approx \frac{3}{4} \cdot \frac{V_{DD}}{I_{DSAT}} \left( 1 - \frac{5}{6} \cdot \lambda \cdot V_{DD} \right)
\]

The Transistor as a Switch

\[ V_{GS} \geq V_T \]

\[
R_{eq} = \frac{1}{2} \int_{t_2}^{t_1} R_{on} (t) \cdot dt = \frac{1}{t_2 - t_1} \int_{t_2}^{t_1} \frac{V_{DS} (t)}{I_D (t)} \cdot dt
\]

\[
R_{eq} \approx \frac{1}{2} \left( R_{on} (t_1) + R_{on} (t_2) \right)
\]
### Transient Response

The transient response of a circuit can be described by the following equation:

\[ t_p = 0.69 \frac{C}{R_{eqn} + R_{eqp}} \]

where:

- \( t_p \) is the transition time
- \( C \) is the total capacitance
- \( R_{eqn} \) is the equivalent resistance when the output is high
- \( R_{eqp} \) is the equivalent resistance when the output is low

### Design for Performance

- **Keep capacitances small**
- **Increase transistor sizes**
  - watch out for self-loading!
- **Increase \( V_{DD} \)**
Delay as a function of $V_{DD}$

$$t_p = \frac{3}{4} \frac{C_L \cdot V_{DD}}{I_{D_{SAT}}} = 0.52 \frac{C_L \cdot V_{DD}}{(W/L)_n \cdot k_n \cdot V_{D_{SAT}}} \cdot (V_{DD} - V_T - V_{D_{SAT}}/2)$$

Device Sizing

Self-loading effect: Intrinsic capacitances dominate
NMOS/PMOS Ratio

\[ \beta = \frac{W_p}{W_n} \]

Impact of Rise Time on Delay

\[ t_p = t_{\text{step}(i)} + \eta t_{\text{step}(i-1)} \]
Power Dissipation

Where Does Power Go in CMOS?

- Dynamic Power Consumption
  - Charging and discharging capacitors

- Short Circuit Currents
  - Short-circuit path between supply rails during switching

- Leakage
  - Leaking diodes and transistors
#1: Dynamic Power Dissipation

- Not a function of transistor sizes!
- Need to reduce $C_L$, $V_{dd}$, and $f$ to reduce power

$$\text{Energy/transition} = C_L \cdot V_{dd}^2$$

$$\text{Power} = \text{Energy/transition} \cdot f = f \cdot C_L \cdot V_{dd}^2$$

Modification for Circuits with Reduced Swing

- Can exploit reduced swing for lower power (e.g., reduced bit-line swing in memory)
Adiabatic Charging

Consider charging a capacitor

\[ V_C = \frac{1}{C} \int_0^T i \cdot dt = \frac{1}{C} \cdot I_{\text{avg}} \cdot T \quad \Rightarrow \quad I_{\text{avg}} = \frac{C \cdot V_C}{T} \]

\[ E_{\text{dis}} = R \int_0^T i^2(t) \cdot dt \geq R \int_0^T \frac{1}{2} I_{\text{avg}}^2 \cdot dt = R \cdot \frac{1}{2} I_{\text{avg}}^2 \cdot T \]

\[ E_R = \frac{1}{2} C \cdot V_C^2 \]

\[ E_R = \frac{R \cdot C}{T} \cdot C \cdot V_C^2 \]

Adiabatic Charging

\[ V_I = R \cdot I + V_C = R \cdot C \cdot \frac{dV_C}{dt} + V_C \]

\[ V_I = \text{const} \quad \text{Exponential current} \]

\[ I = I_{\text{avg}} \quad \text{Linear ramp on } V_I \]

\[ E_R = \frac{1}{2} C \cdot V_C^2 \]

\[ E_R = \frac{RC}{T} \cdot C \cdot V_C^2 \]

\[ \text{wins if } T > 2RC \]
Node Transition Activity and Power

- Consider switching a CMOS gate for \( N \) clock cycles

\[
E_N = C_L \cdot V_{dd}^2 \cdot n(N)
\]

\( E_N \): the energy consumed for \( N \) clock cycles
\( n(N) \): the number of \( 0 \rightarrow 1 \) transitions in \( N \) clock cycles

\[
P_{\text{avg}} = \lim_{N \to \infty} \frac{E_N}{N} \cdot f_{\text{clk}} = \left( \lim_{N \to \infty} \frac{n(N)}{N} \right) \cdot C_L \cdot V_{dd}^2 \cdot f_{\text{clk}}
\]

\[
\alpha_{0 \rightarrow 1} = \lim_{N \to \infty} \frac{n(N)}{N}
\]

\[
P_{\text{avg}} = \alpha_{0 \rightarrow 1} \cdot C_L \cdot V_{dd}^2 \cdot f_{\text{clk}}
\]

#2: Short-Circuit Currents

![Short-Circuit Currents Diagram]

\[
I_{\text{SC0}} = f(V_{\text{in}})
\]

- \( V_{\text{in}} \): input voltage
- \( V_{\text{out}} \): output voltage
- \( V_{dd} \): supply voltage
- \( C_L \): load capacitance

<table>
<thead>
<tr>
<th>( V_{dd} ) (mA)</th>
<th>( V_{\text{in}} ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.15</td>
<td>0.00</td>
</tr>
<tr>
<td>0.10</td>
<td>0.05</td>
</tr>
<tr>
<td>0.10</td>
<td>1.00</td>
</tr>
<tr>
<td>0.15</td>
<td>2.00</td>
</tr>
<tr>
<td>0.10</td>
<td>3.00</td>
</tr>
<tr>
<td>0.10</td>
<td>4.00</td>
</tr>
<tr>
<td>0.15</td>
<td>5.00</td>
</tr>
</tbody>
</table>
How To Keep Short-Circuit Currents Down?

Short circuit current goes to zero if \( t_{\text{fall}} \gg t_{\text{rise}} \)
but can’t do this for cascade logic, so ...

Minimizing Short-Circuit Power

- Keep the input and output rise/fall times the same
  (<10% of total consumption)

  From: Veendrick, IEEE Journal of Solid-State Circuits, Aug’84

- If \( V_{dd} < V_{Tn} + |V_{Tp}| \) then short-circuit power can be eliminated!
#3: Leakage

Sub-threshold current is one of the most compelling issues in low-energy circuit design!

Reverse-Biased Diode Leakage

\[ I_{DL} = J_S \times A \]

\[ J_S = 10-100 \text{ pA/\mu m}^2 \text{ at 25 deg C for 0.25\mu m CMOS} \]

\[ J_S \text{ doubles for every 9 deg C!} \]
**I_D versus V_GS**

The graph shows the relationship between I_D (current) and V_GS (gate-source voltage) for both long and short channel devices. The curves are labeled as quadratic and linear, indicating different behaviors at varying voltages.

**Sub-Threshold Conduction**

The Slope Factor S is defined as \( \Delta V_{GS} \) for \( I_{D2}/I_{D1} = 10 \). The equation for the slope factor is given by:

\[
S = n \left( \frac{kT}{q} \right) \ln(10)
\]

Typical values for S: 60 – 100 mV/decade.
Sub-Threshold Leakage Component

- Leakage control is critical for low-voltage operation

\[ I_D = I_0 e^{\frac{qV_{DS}}{nkT}} \left( 1 - e^{\frac{-qV_{DS}}{kT}} \right) \]

Sub-Threshold \( I_D \) vs. \( V_{GS} \)

\( V_{DS} \) from 0 to 0.5V
Sub-Threshold $I_D$ vs. $V_{DS}$

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{nkT}}\right) (1 + \lambda \cdot V_{DS})$$

$V_{GS}$ from 0 to 0.3V

Hw3, Prob4

$n=1.5$

$kT/q = 26\text{mV}$

#4: Static Power Consumption

$$P_{stat} = P(\text{in}=1) \cdot V_{dd} \cdot I_{stat}$$

Wasted energy ...

Should be avoided in most cases, but could help reducing energy in others (e.g. sense amps)
Principles for Power Reduction

- **Prime choice: Reduce voltage!**
  - Recent years have seen an acceleration in supply voltage reduction
  - Design at very low voltages still open question (0.6 … 0.9 V by 2010!)

- Reduce switching activity

- Reduce physical capacitance

The Sub-Micron MOS Transistor

- Threshold Variations

- Sub-threshold Conduction

- Parasitic Resistances
Threshold Variations

- **Long-channel threshold**
  - Threshold as a function of channel length (for low $V_{DS}$)

- **Low $V_{DS}$ threshold**
  - Drain induced barrier lowering (DIBL) (for low $L$)

Next Lecture

- Optimizing for Performance and Power