1)

a)

<table>
<thead>
<tr>
<th>Point</th>
<th>$V_{in}$ (V)</th>
<th>$V_{out}$ (V)</th>
<th>PMOS</th>
<th>NMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.00</td>
<td>2.28</td>
<td>Linear</td>
<td>saturation</td>
</tr>
<tr>
<td>C</td>
<td>1.50</td>
<td>0.153</td>
<td>saturation.</td>
<td>Linear</td>
</tr>
<tr>
<td>D</td>
<td>1.81</td>
<td>0.0253</td>
<td>saturation</td>
<td>Linear</td>
</tr>
</tbody>
</table>

b) and d)

<table>
<thead>
<tr>
<th>N</th>
<th>f</th>
<th>Nf</th>
<th>N(1+f)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>3.68</td>
<td>11.05</td>
<td>14.05</td>
<td>We use 3 stage buffer for room temperature</td>
</tr>
<tr>
<td>4</td>
<td>2.66</td>
<td>10.64</td>
<td>14.64</td>
<td>we use 4 stage buffer for 4 K</td>
</tr>
</tbody>
</table>

c)

VTC does not change much. Because $k'$ for PMOS and NMOS both increase by 50 %, so VTC does not shift to right or left, and capacitance change does not affect DC properties. You will not lose any points if you point out that the VTC looks a little bit sharper.

2)

a)

$V_{AA,L}=0$

$V_{AH}=2.29$

$$k \cdot \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right) = 100 \mu A \quad V_{DS} = VDD - V_{AH}$$

b)

$V_{BH}=VDD$

$V_{BL}=0.27$

$$k_n \cdot \frac{W}{L} \left( (V_{GS} - V_T) V_{BL} - \frac{1}{2} V_{BL}^2 \right) = \frac{2.5 - V_{BL}}{10K\Omega}$$

c)

$$\tau_{pHL} = (R_p \parallel R_0) C_L$$

$$\tau_{pHL} = (R_N \parallel R_0) C_L$$
\[ R_p = \frac{1}{2} \left( \frac{2.5 - 0.27}{k'W/L((V_{DD} - V_T)V_{DSAT} - \frac{1}{2}V_{DSAT}^2)} \right) + \frac{2.5 - 1.25}{k'W/L((V_{DD} - V_T)V_{DSAT} - \frac{1}{2}V_{DSAT}^2)} \right) = 4.5 \Omega \]

\[ R_S = \frac{3}{4} \frac{V_{DD}}{I_{sat}(V_{AH})} = 4.2 \Omega \]

The factor is not 0.69!! It is \( \ln\left(\frac{V_{BL} - V_{DD}}{V_{DD}/2 - V_{BL}}\right) = 0.58 \) for low to high and \( \ln\left(\frac{V_{DD} - V_{BL}}{V_{DD}/2 - V_{BL}}\right) = 0.83 \) for high to low.

\[ t_{pHL} = 0.83 \times (4.2 \parallel 10)k \times 12 f = 29.5 \, ps, t_{pLH} = 0.58 \times (4.5 \parallel 10)k \times 12 f = 21.6 \, ps \]

So, \( t_p = \frac{1}{2} (29.5 \, p + 21.6) = 25.5 \, ps \)

3,

a) Same equivalent pull-up resistance, same load capacitance, so the ratio is 1.
b) Figb has twice larger resistance as Fig2, so the ratio is 1/2.
c) Total power ratio depends on the total capacitance.
\[ \frac{6 + (6 + 6) \times 3 + 6}{6 + (6 + 8) \times 3 + 6} = \frac{6}{7} \]
d) DIBL effect, smaller VDS make VT larger so less leakage.