EECS 141: FALL 2006—MIDTERM 2

For all problems, you can assume the following transistor parameters (unless mentioned otherwise):
 NMOS: 
 \( V_{th} = 0.4, \quad k_n = 115 \, \mu A/V^2, \quad V_{dsat} = 0.6 \, V, \quad \lambda = 0, \quad \gamma = 0.4 \, V^{1/2}, \quad 2\Phi_F = -0.6 \, V \)
 PMOS: 
 \( V_{tp} = -0.4 \, V, \quad k_p = 30 \, \mu A/V^2, \quad V_{dsat} = -1 \, V, \quad \lambda = 0, \quad \gamma = -0.4 \, V^{1/2}, \quad 2\Phi_F = 0.6 \, V \)

NAME

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GRAD/UNDERGRAD

Solution

Problem 1: ____/18
Problem 2: ____/10
Problem 3: ____/22
Total: ____/50
PROBLEM 1. Logic Gates (18 points)

In this problem, we will implement a logic gate in static complementary CMOS. The pull-up network of this gate is shown in Figure 1. Note that, input $D$ is the one that is the last arriving and is placed closest to the output, $Y$.

![Figure 1.](image)

a) (4 pts) Complete the Figure 1 to form a complementary static CMOS gate.
b) (4 pts) Can the layout of the gate from part a) be implemented using continuous stripes of diffusion? Explain your answer.

No it cannot since there is no Euler Path for the Pull-up Network

* we gave full-credit if you re-drew the schematic and answered "yes"
c) (6 pts) Size the gate such that the \( t_{PHL} \) is equal to \( t_{PLH} \), and equals the propagation delay of a unit-sized inverter \( (W_n = 1 \text{ unit}, W_p = 2 \text{ units}) \) in the worst case, under a condition that all inputs have the same capacitance.

\[
1 + x = 2 + y \rightarrow x = 1 + y \\
\frac{1}{x} + \frac{1}{x} + \frac{1}{y} = \frac{1}{2} \\
x = 6.37 \\
y = 5.37
\]

d) (4 pts) If input D is the only one that is critical (late arriving), how would you change the schematic and/or layout of this gate to reduce the delay, without changing transistor sizing?

- we should switch the positions of "B/C" pmos with "A" pmos, yielding a

\[
\text{This way we can get a layout without diffusion breaks.}
\]

- input D is already in the optimal position and should be kept as is.
PROBLEM 2. Pass-Transistor Logic (10 points)

A pass-transistor implementation of a logic function $Y$ is shown in Figure 2.

Figure 2.

a) (4pts) What is the logic function implemented by the gate in Figure 2?

$$Y = A \cdot B \cdot C$$
b) (6pts) Complete the schematic from Figure 2, so it implements the function in the complementary pass transistor logic style (that is the NMOS-only style with complementary inputs and complementary outputs).

\[ \overline{Y} = \overline{A} \overline{B} \cdot \overline{C} = \overline{A} + \overline{B} + \overline{C} \]

Other correct solutions exist and were given full credit.
PROBLEM 3. Minimizing delay (22 points)

A combinational logic block is shown in Figure 3. All inputs arrive at the same time. Input capacitance of all inputs is 6fF and the output load is 60fF. All gates are symmetrically sized. In this technology, gate capacitances equal drain capacitances ($\gamma = 1$).

a) (6pts) Find the logical effort and the intrinsic delay for each of the logic gates: INV, NAND3 and NOR2.

\[ \text{INV:} \quad P = 1, \quad G = 1 \]
\[ \text{NAND3:} \quad P = 3, \quad G = \frac{5}{3} \]
\[ \text{NOR2:} \quad P = \frac{6}{3} = 2, \quad G = \frac{5}{3} \]
b) (10pts) Determine the capacitances per input of each of the gates in Figure 3, along the critical path, to minimize the delay.

\[ C_C = \frac{60 \times \frac{5}{3} \times 1}{4.37} = 22.9 \text{ fF} \]
\[ C_B = \frac{22.9 \times 1 \times 1}{4.37} = 5.24 \text{ fF} \]
\[ C_A = \frac{5.24 \times 3 \times \frac{5}{3}}{4.37} = 6.05 \text{ fF} \]

\[ F = \frac{60}{6} = 10. \]
\[ B = 1 \times 3 \times 1 = 3 \]
\[ G = \frac{5}{3} \times 1 \times \frac{5}{3} = \frac{25}{9} \]
\[ H = 10 \times 3 \times \frac{25}{9} = \frac{250}{3} \]
\[ h = \frac{3 \sqrt{\frac{250}{3}}}{3} = 4.37 \]

\[ G = \frac{5}{3} \times \frac{25}{9} + \frac{22.9}{5.24} = \frac{5}{3} \times \frac{b}{6f} + \frac{22.9}{b} \]

\[ \times \text{ two solutions exist since } b \text{ can be made a certain amount larger or smaller from the optimal size to slow down the circuit. Naturally, the smaller size is preferred since it reduces area and power consumption}. \]

\[ b = 28.57 \text{ or } 2.89 \]

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