Problem #1: Power in CMOS

Let’s evaluate the effect of logic choice on power dissipation. Circuit A is an AND4 implemented as a NAND2 chain while Circuit B implements the same function using a 4 input gate.

a) Size circuit A and circuit B for minimum delay with Cin of 3fF and Cout of 50fF. Report your answer in terms of the input capacitance seen at each gate.

b) Given that \( P(A=1) = P(B=1) = P(C=0) = P(D=0) = 0.25 \), calculate the probability of energy consuming transitions \( P(0 \rightarrow 1) \) at the outputs of the gates in both circuits.

c) Assuming both circuits are operating at 1 GHz, calculate the dynamic power consumption of the circuit. Assume \( \gamma = 1 \), \( V\text{dd} = 2.5V \), and only consider capacitances at the inputs and output of the gates.
Problem #2: Schmitt Trigger

The circuit on the following page is a pseudo-NMOS Schmitt trigger. Assume that the PMOS transistor remains in saturation over entire range of operation. $V_{dd} = 1.5V$, $V_{tn} = V_{tp} = 0.4V$, $k_n = 115\mu A/V^2$, $k_p = 30\mu A/V^2$

a) Compute $V_{OH}$ and $V_{OL}$.

b) Compute the switching points $V_{M^+}$ (for input making low-to-high transition) and $V_{M^-}$ (for the input making a high-to-low transition).

c) Sketch the VTC. Compare results with SPICE simulations. In particular, you should obtain different VTC curves for high-to-low transitions and low-to-high transitions. Perform a transient analysis with the following as input: - Vtest vin 0 PWL 0 0 50n 0 100n Vdd 150n Vdd 200n 0
Problem #3: Pulse-triggered latch

Figure above shows a practical implementation of a pulse-triggered latch. Clock Clk is ideal with 50% duty cycle.

Data: \( t_{\text{p,inv}} = 200\text{ps}, \ Clkd = 10\text{fF}, \ Cx = 10\text{fF}, \ CQ = C\overline{Q} = 20\text{fF} \)

a) Draw the waveforms at nodes Clk, Clkd, X and Q for two clock cycles, with D equals 0 in one cycle and 1 in the other.

b) Are the setup and hold times positive, negative, or approximately zero?

c) If the probability that D will change its logic value in one clock cycle is \( \alpha \), with equal probability of being 0 or 1, what is the power consumption of this circuit? (excluding the power consumption in the clock line) Assume \( f_{\text{clk}} = 100 \text{ MHz} \).